SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section describes the theory of operation of the major subassemblies of the Ampex 210 terminal.

4.2 GENERAL DESCRIPTION

The basic block diagram in Figure 4-1 illustrates signal flow between the subassemblies of the terminal. The following paragraphs discuss the interfacing of subassemblies.

4.3 OPERATION AND COMPONENTS OF THE TERMINAL CONTROLLER PWBA

The hardware and circuitry of the controller PWBA is composed of the major functional blocks, input/output mapping, and interface buses, shown in Figure 4-2.

Functional sections of the terminal are controlled by the Central Processing Unit (CPU) via a system data bus, an address bus, and control lines. Display and communications sections have some circuitry that run independently of the CPU. The display section, for example, refreshes video continuously and automatically once initiated by the CPU.

The host computer communicates with the terminal via an RS232C interface. The CPU receives serial data from the keyboard via a keyboard interface circuit resident in the Cathode Ray Tube (CRT) controller chip.

The CPU is a Z80A microprocessor with fully-enhanced 8080-like instruction set. The hardware, as designed, uses Input/Output (I/O) instructions to access the I/O ports.

There are two interrupt sources. The maskable interrupt is generated by an ACIA (Asynchronous Communication Interface Adapter) chip and the non-maskable interrupt is generated by a PVTC (Programmable Video Timing Controller) chip.

The data/address buses and control lines allow the CPU to access the program ROM, the scratch pad RAM, and all of the I/O ports. Depending on firmware requirements, 16K to 24K bytes of program P/ROM can be installed.

The CPU's scratch-pad and data memory consists of a 2K x 4 CMOS RAM and provides nonvolatile storage of all of the set-up parameters including operational modes, communication parameters, emulation parameters, etc., through the use of a 3V lithium battery.

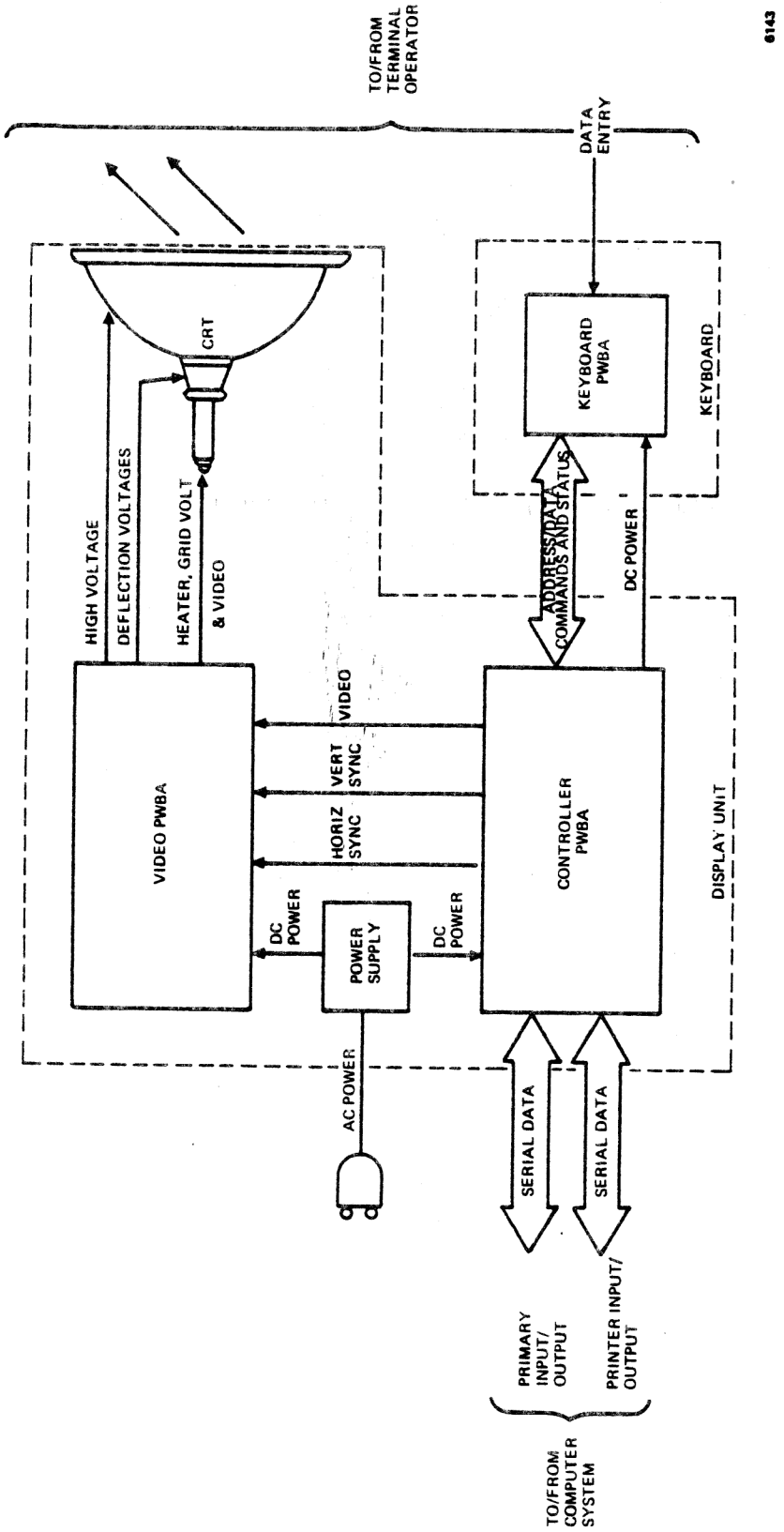


Figure 4-1. Terminal Basic Block Diagram

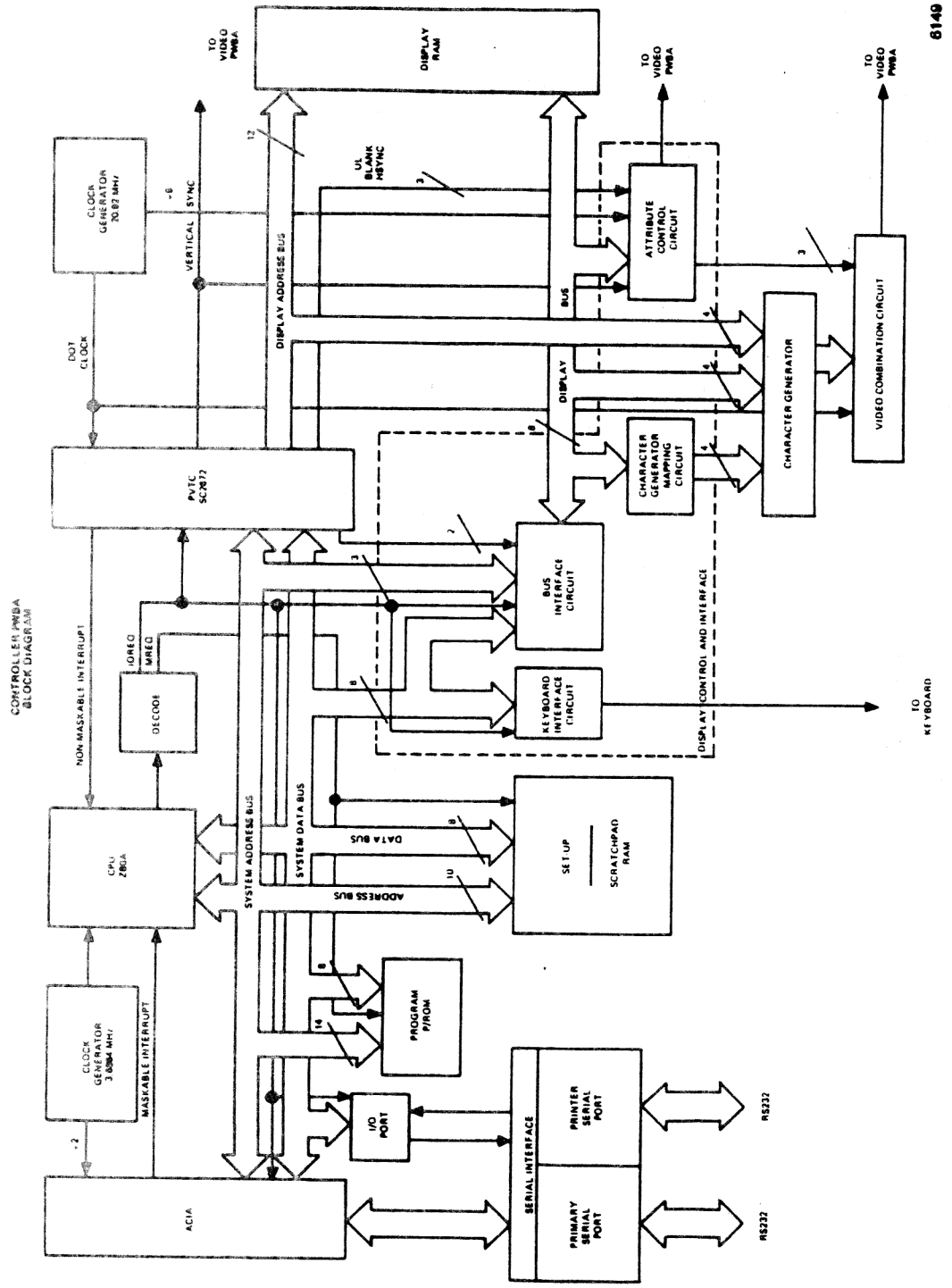


Figure 4-2. Controller PWBA Block Diagram

4.3.1 Input/Output Mapping And The CPU

Through I/O mapping, the CPU interfaces with:

- PVTC chip
- ACIA chip and other communications-related circuitry
- Keyboard (via the CRT controller chip)
- CRT controller chip

4.3.1.1 Display I/O

Display I/O gives the CPU control over the PVTC chip (including initializing the PVTC chip, reading/writing cursor position, flashing clock, and scrolling).

Once initialized by the CPU, the PVTC chip subsequently performs the continuous refreshing required of the PVTC by generating the video, horizontal drive, and vertical sync signals required by the CRT monitor.

4.3.1.2 Communication I/O

The communication I/O gives the CPU control over the ACIA chip (including sending/receiving characters on the word level, checking ACIA status and BREAK control) and other communications circuitry (including primary/printer port selection and bidirectional/ extension printer port selection).

Once initialized by the CPU, the ACIA chip and other communications circuitry subsequently perform the parallel-to-serial, serial-to-parallel, and signal level conversions required for serial port interfacing.

4.3.1.3 Keyboard I/O

The keyboard I/O allows the CPU via the CRT controller chip to transmit and receive data to and from the keyboard.

4.3.2 Central Processing Unit

The CPU is the control center of the terminal controller. The following paragraphs describe the functions of the CPU, the buses, and memory interfaces used to control other parts of the system.

4.3.2.1 Functions of the CPU

As mentioned earlier, the CPU is a Z80A microprocessor. It contains circuitry for program execution as well as the program registers:

Clock - The CPU clock is a 3.6864 MHz generated from a 3.6864 MHz crystal. The clock input to the Z80 requires the special high level generation by a 74L1S04 driver (U2-8, 9) and a 330 ohm resistor.

Reset - The CPU is reset by the power-up reset circuit or by pressing SHIFT/BREAK twice.

Memory Request (MREQ) - At the beginning of each cycle, an MREQ is issued. The MREQ is used to enable the decoding circuitry (U28) to generate chip select signals.

Read/Write Signals - Following the MREQ for each memory or memory-mapped I/O read/write cycle, a Bus read or write signal occurs when a byte is to be read from or written to memory or memory-mapped I/O.

Input/Output Request (IORQ) - The IORQ is used to enable the I/O port function.

Maskable Interrupt - Maskable interrupt of the CPU is generated by the ACIA chip. There are two possible causes of maskable interrupts: Receive Data Register Full or Transmit Data Register Empty.

Non-maskable Interrupt - Non-maskable interrupt input of the CPU is generated by the PVTC chip. There are two possible causes of non-maskable interrupts: Vertical Blank or Line Zero.

Wait - The wait input signal allows the CPU to wait for slower responses of read and write accesses to the ACIA chip.

4.3.2.2 Buses Used For Interfacing

During the CPU's read memory or write memory, the Data/Address bus signal lines carry address information to the other components.

Data Bus - The CPU's eight data lines, D7 through D0, carry the data between the CPU and all of the memories and I/O devices.

Address Bus - There are sixteen address lines, A0 through A15, used to address the memories and I/O ports. In general, the lower address lines are used to address specific bytes in the program P/ROM, and the data RAM. The highest address bits select between the system entities.

4.3.2.3 Memory Interfaces

The following paragraphs contain descriptions of the various memory interfaces:

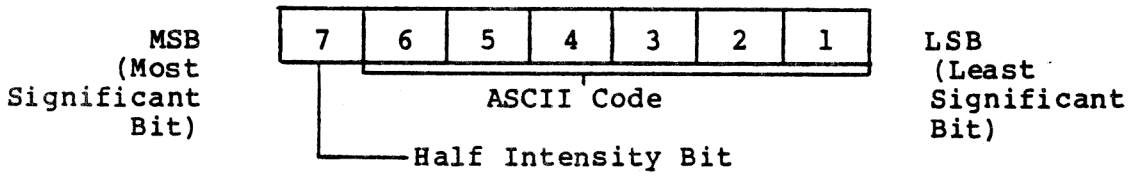
Program ROM/PROM - The program instruction memory can be configured out of various types of numbers of ROMs/PROMs. The total memory space is 24K. Table 4-1 shows the various jumper settings and IC (Integrated Circuit) locations for select memory capacity.

Table 4-1. Program Instruction Memory Configurations

Total Memory	Jumper Settings	Address Ranges For Access	IC Location	IC Location	Memory For Each IC
16K	W15-W16 W11-W13 W8 -W9	0-1FFF 2000-3FFF	U23 U22	2764/2364 2764/2364	8K 8K
20K	W14-W15 W11-W12 W9 -W10	0-3FFF 4000-4FFF	U23 U22	27128/23128 2732/2332	16K 4K
24K	W14-W15 W11-W12 W9 -W10	0-3FFF 000-5FFF	U23 U22	27128/23128 2764/2364	16K 8K

Data RAM - The CPU's general purpose data RAM consists of a 2K x 8 bytes static CMOS random-access memory. The data RAM is split into two different regions. The region from 8000H to 803FH is used as software switches to define the terminal's default states. The region from 8040H to 87FFH is used as the CPU's scratch-pad RAM.

Display RAM - The display RAM consists of one page holding 2000 character positions. Each character contains 8 bits:



The seven least significant bits contain the ASCII character code that is displayed for that character position. The firmware will typically implement Bit 7 as the protect bit, causing the character to be displayed in half intensity, and is treated by the hardware as one attribute bit.

If the four most significant bits of a character are 1001, then the hardware treats this as an attribute delimiter. If the bit corresponding to the delimiter is set to "1", then the appropriate attribute will be activated. Table 4-2 defines each bit of an attribute delimiter.

Table 4-2. Attribute Delimiter Bits

Bit	Definition
3	Underscore
2	Reverse video
1	Blink (half intensity for ADM 5)
0	Blank (security)

Transfer of data between the CPU and the display RAM is accomplished via the memory interface circuit resident in the CRT controller chip and is controlled by the PVTC signals: Read Data Buffer and Write Data Buffer.

4.3.3 Operation of CPU Memory

The general theory of operation of the hardware for the program memory is described in the following paragraphs.

4.3.3.1 Program ROM/PROM

The program ROM/PROMs are static and begin their access time as soon as the address lines are valid (i.e., they access continuously). The ROM/PROM drive the main data bus directly so that the access time from address valid to data out is 350 ns, maximum. The upper memory address bits are used to select and enable the specific ROM/PROM's data outputs using pin 20 of the selected IC.

4.3.3.2 Data RAM

The permanent 2K bytes of CMOS RAM (U25) are used as CPU scratch-pad memory and addressed from 8000H to 87FFH.

The CMOS is used together with a long life (10 years minimum) 3.4V lithium battery for nonvolatile storage of modes of operation. The CMOS RAM write enable pin goes directly to the CPU's WR pin (U24-22). When AC power is off, the CMOS RAM will draw standby current from the 3.4V battery. When AC power is on, the CMOS RAM will draw current from the +5V supply.

4.4 OPERATION OF DISPLAY CIRCUITRY

The following paragraphs discuss the operation of the programmable video timing controller and display circuitry. Figure 4-3 is a block diagram of the Video PWBA.

4.4.1 General Information

The characters being displayed on the CRT screen are accessed (read and written) by the CPU via the display RAM. This memory consists of one page of 1920 bytes and a status line of 80 bytes. Bit 7 of the display RAM determines the half-intensity attribute. The other bits constitute the ASCII codes. But the codes from 10H to 1FH are used as attribute delimiters.

The display RAM requires that the Programmable Video Timing Controller (PVTC) be properly controlled by the CPU for transferring data to and from the display RAM.

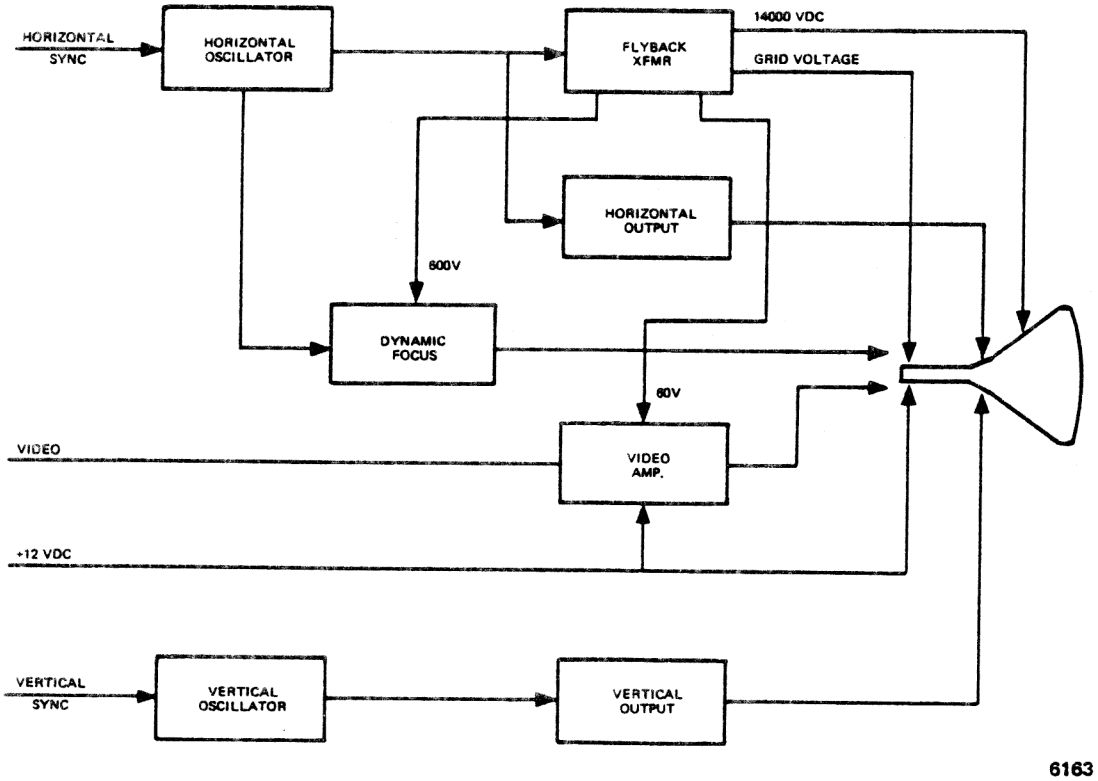


Figure 4-3. Video PWBA Block Diagram

4.4.2 Operation of the PVTC Chip

The Programmable Video Timing Controller (PVTC) chip is accessed by three control strobes: Chip enable, CPU read, and CPU write signals. The 00H decode output of the upper address lines provide the chip select for the PVTC. The lower three address lines (A0-A2) and read/write signals go to the PVTC chip for initialization register selection.

Table 4-3 provides the PVTC chip initialization register selection.

Table 4-3. PVTC Chip Initialization Register Selection

INITIALIZATION REGISTERS	VALUE (IN HEX) 60 Hz	65 Hz
IR0	58	58
IR1	25	25
IR2	1B	1B
IR3	90	2A
IR4	18	18
IR5	4F	4F
IR6	0B	0B
IR7	2B	2B
IR8	01	01
IR9	10	10
IR10	98	98

4.4.3 Initialization Register Parameters

Parameters of the initialization register values indicated in Table 4-3 are:

Initialization Register 0 (IR0)

Bit 7, not used (=0)
Bits 6 - 3 = N Scan lines/character row (where scan lines/character row = N + 1)
Bit 2 = 0; sync select (VSYNC)
Bit 1 - 0 = 00; buffer mode select (independent mode)

Initialization Register 1 (IR1)

Bit 7 = 0; non-interlace
Bits 6 - 3 =N; equalizing constant (where equalizing constant = N + 1)

Initialization Register 2 (IR2)

Bit 7 not used (=0)
Bits 6 - 3 =N; horizontal sync width (where horizontal sync width = .2*N+2)
Bit 2 = T; horizontal back porch (where horizontal back porch = 4*T+1)

Initialization Register 3 (IR3)

Bits 7 - 5 =N; vertical front porch (where vertical front porch = 4*N+4)
60 Hz: vertical front porch = 4*4+4 = 20 (scan lines)
65 Hz: vertical front porch = 4*1+4 = 8 (scan lines)
Bits 4 - 0 =T; vertical back porch (where vertical back porch = 2*T+4)
60 Hz: vertical back porch = 2*16+4 = 36 (scan lines)
65 Hz: vertical back porch = 2*8+4 = 20 (scan lines)

Initialization Register 4 (IR4)

Bit 7 = 0; character blink rate = 1/16 VSYNC
Bits 6 - 0 = N; character row/screen (where character row/screen = N + 1)

Initialization Register 5 (IR5)

Bit 7 - 0 = N; character/row (where character/row = N + 1)

Initialization Register 6 (IR6)

Bits 7 - 4 = N; first line of cursor (scan line 0)
Bits 3 - 0 = T; last line of cursor (scan line 11)

Initialization Register 7 (IR7)

Bits 7 - 6; not used (=0)
Bit 5 = 1; cursor blinking
Bit 4 = 0; normal size character
Bits 3 - 0 = N; underline position (scan line 11)

Initialization Register 8 (IR8)

Bits 7 - 0 = display buffer first address Least Significant Bits

Initialization Register 9 (IR9)

Bits 7 - 4 = N; display buffer last address (where display buffer last address = 1024xN+1023)
Bits 3 - 0 = display buffer first address Most Significant Bits = 0

Initialization Register 10 (IR10)

Bit 7 = 1; cursor blink rate = 1/32 VSYNC
Bits 6 - 0 = N; split screen interrupt row = 18 (H)

4.4.4 Valid Address/Blanking And Sync Signals Relationship

Figure 4-4 illustrates the timing of a frame showing the relationship between the valid character address (for the twenty-five 80-character rows) and the blanking and sync signals. The left and right edges correspond to the start of the horizontal sync and the top and bottom edges correspond to the start of the vertical sync.

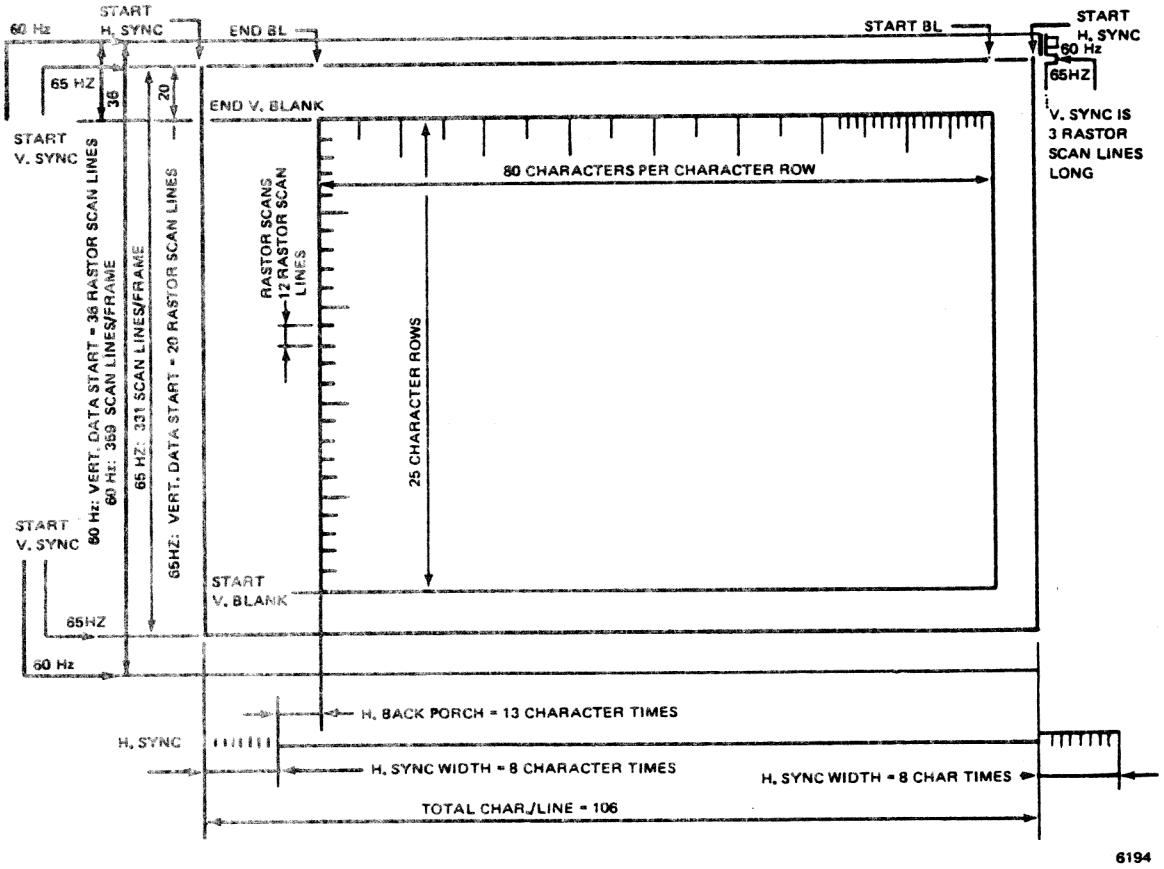


Figure 4-4. PVTC Chip Timing Frame

The inner solid-lined rectangle (twenty-five 80-character rows) represents the time during which the PVTC chip outputs valid address on DADD0-DADD10, LA0-LA3. The DADD0-DADD10 lines go from zero to 79 on each scan across the 80-character positions and count out the 25 character rows, covering rows 0 through 24 on each frame (the starting and ending counters programmatically changed using the screen start character row address control command). LA0-LA3 generate one scan line per character row, covering all 25 rows on each frame.

The positive-true blanking signal is emitted with no character time delays after the end of the last character (80th character) to the beginning of the first character address, as well as continuously from the end of the last character row until the beginning of the first character row.

4.4.4.1 Horizontal Sync

The horizontal sync (HSYNC) is delayed by five characters (as blanking, above) and additionally has a "back porch" of thirteen characters after the HSYNC ending. The HSYNC signal width is ten characters long.

4.4.4.2 Vertical Sync

The vertical sync (VSYNC) starts after the last scan line of the frame and continues for three horizontal scan lines. The programming of the total scan lines per frame determines whether there are 60 or 65 frames per second. Following the last scan line (at the same time the VSYNC starts), the vertical character row start is delayed by 36 scan lines for 60 Hz and 20 scan lines for 65 Hz. This variation provides for approximately the same vertical centering for both 60 Hz and 65 Hz.

4.4.4.3 Cursor Signal

The cursor signal is emitted during the time when the internal cursor address matches the screen address (DADD0-DADD10).

4.5 OPERATION OF THE DISPLAY RAM

Displayed characters and attribute control characters are stored in and received from either of two S/RAMs. The PVTC chip generates three control signals: Buffer Chip Enable, Write Data Buffer, and Read Data Buffer. These signals provide the transfer of data between the CPU and the display S/RAMs (via the interface circuits resident in the the CRT controller chip).

4.6 CHARACTER GENERATOR

The four least significant address bits of the character generator are derived from the scan line address bits of the PVTC chip. During actual display, the 7 ASCII bits address a "character generator ROM" which allows the specifications of a 7 x 10 dot matrix to be displayed within the 9 x 12 field as shown below. Thus, each 8-bit data word can select any one of 256 character-generated ROM patterns to fill in the 7 x 10 dot matrix.

The display character field has the following format:

	COLUMN									
ROW	0	1	2	3	4	5	6	7	8	
0	X	X	X	X	X	X	X	X	X	Blank*
1	X	A	A	A	A	A	A	A	X	Top Scan Row
2	X	A	A	A	A	A	A	A	X	Character Scan Row
3	X	A	A	A	A	A	A	A	X	"
4	X	A	A	A	A	A	A	A	X	"
5	X	A	A	A	A	A	A	A	X	"
6	X	A	A	A	A	A	A	A	X	"
7	X	A	A	A	A	A	A	A	X	"
8	X	A	A	A	A	A	A	A	X	"
9	X	A	A	A	A	A	A	A	X	"
10	X	A	A	A	A	A	A	A	X	Bottom Scan Row
11	-	-	-	-	-	-	-	-	-	Blank (except graphics and underline)**

*Row 0 is always blank, except for graphics.
**Row 11 is always blank, except for graphics and underlines.

4.7 GENERATION OF VIDEO SIGNALS

At the end of each character generator access, the dot data are loaded into a shift register in order to begin displaying the scan line of the character. The basic video "dots" emanate from the shift register.

4.7.1 Basic Video

For normal (non-graphics) characters, the first and last dot positions are always blanked. For graphics characters, the first dot position has the same value as the next dot position and the last dot position has the same value as the previous dot position. This allows the horizontal line graphics characters to extend all the way to the adjacent character fields for producing multicharacter solid horizontal lines.

If blank video is desired, the video "dots" will be blanked. If reverse video is desired, the video "dots" will be driven onto a two-level video point where there is half or full intensity before being driven onto the monitor for display.

4.7.2 Attribute Control Signals

The half intensity attribute bit becomes active as the shift register is loaded. The attribute bit is held constant throughout the display character's dots for the scan line in progress. The half intensity bit, when on, causes the two-level video point to be loaded down, thus lowering the video intensity level. Attribute bits will remain constant until another attribute bit delimiter is encountered.

The inverse video bit complements the video polarity. It is effective following character and scan line blanking controls to reverse the background intensity level. The blank attribute bit blanks the character's video level causing the bit to go to the background level. The blinking bit causes the video to alternate between the normal and blanked-to-background states. This blinking rate is under program control.

4.8 OPERATION OF SERIAL INTERFACE CIRCUITRY

The R6551A Asynchronous Communication Interface Adapter (ACIA) chip provides a program-controlled interface between the 8-bit microprocessor-based systems and serial communication data sets. With its on-chip baud rate generator, the ACIA is capable of transmitting and receiving different program-selectable rates between 50 and 19.2K bits per second.

4.9 DRIVER-RECEIVER OPERATION

The primary and auxiliary (printer) ports receive on RS232 lines.

4.9.1 Primary Port

When the primary port is selected, it can transmit on an RS232 circuit. Table 4-4 lists the signal definitions and connector pins of the RS232 primary serial interface port.

Table 4-4. RS232 Pin Assignments and Signal Definitions

PIN	RS232 CIRCUIT	DEFINITION
1	AA	Protective Ground
2	BA	Transmit Data to Modem/Host
3	BB	Receive Data from Modem/Host
4	CA	Request-to-send
5	CB	Clear-to-send
6	CC	Data Set Ready
7	AB	Signal ground
20	CD	Data Terminal Ready

4.9.2 Printer Port

The printer port's data and control signals are directly connected to the primary port. This allows the printer port to function as a bidirectional printer port.

4.10 OPERATION OF KEYBOARD INTERFACE

The keyboard interface circuitry uses two shift registers to convert the serial data to parallel data. The clock of shift registers is derived from a sixteen-divided counter from HSYNC. The counter starts counting from VSYNC and stops when 12 data bits are received. Since the data stored in the shift register will clear as VSYNC occurs, the CPU should read the data before then and answer the keyboard by accessing the appropriate I/O port.

SECTION V

MAINTENANCE

5.1 INTRODUCTION

This section contains maintenance information for the Ampex 210 Video Display Terminal. Corrective action for field repair of the terminal should be limited to removal and replacement of subassemblies (Section VI). Procedures involving maintenance adjustments and repairs should be performed by service personnel familiar with data terminal and video equipment.

WARNING

Exercise caution while working on the energized video or power supply sections. Avoid physical contact with high voltage leads and connections.

5.2 TEST EQUIPMENT

A list of test equipment (equivalent items may be substituted) for use during adjustment and troubleshooting is provided in Table 5-1. In addition to the items listed, hand tools commonly used in the repair of electronic equipment will be required.

Table 5-1. Test Equipment

Test Equipment	Manufacturer	Model or Part No.
AC Current Probe	Tektronix	P6021
Termination for AC Current Probe	Tektronix	011-0105-00
Oscilloscope	Tektronix	485B
Digital Voltmeter	Fluke	8020A

5.3 PERFORMANCE TESTING

The procedures described below can provide an evaluation of terminal performance.

5.3.1 Power On Self Test

1. Detach the interface cables connected to the primary port and printer port.
2. Apply power to the terminal. Verify the following:
   a. Alarm (beep) sounds within 5 seconds.
   b. Status line and cursor appear within 15 seconds.
   c. No bad component error messages are indicated on the status line. Bad component error messages are explained in Table 5-2.

Table 5-2. Bad Component Error Messages

Message	Explanation	Corrective Action
CMOS CK ERROR	CMOS CHECK SUM FAILURE	Replace Controller PWBA
DATA RAM ERROR	DATA MEMORY FAILURE	Replace Controller PWBA
DISPLAY RAM ERROR	DISPLAY MEMORY FAILURE	Replace Controller PWBA
ROM ERROR	PROGRAM MEMORY FAILURE	Replace Controller PWBA

NOTE: Clear bad component error indicators with SHIFT/BREAK BREAK.

5.3.2 Test Pattern

1. Apply power to the terminal.
2. Place the terminal in local mode (enter Set-Up mode if necessary).
3. Enter ESC V to generate a test pattern (or press the number "1" key while in Set-Up mode).

4. Verify the following:

   a. The terminal's model number and firmware revision level are displayed on line 1.

   b. Reverse video, half intensity, underlining, and flashing character visual attributes are displayed.

   c. All alphanumeric characters, national characters and symbols, and monitor mode facsimile symbols are displayed.

   d. Line graphics are displayed.

5.3.3 Keyboard Test

1. Apply power to the terminal or press SHIFT/BREAK BREAK to reset the terminal if power is already on.

2. Place the terminal in local mode (enter Set-up mode).

3. Starting at the upper left corner of the keyboard, press each symbol, number, and letter key (shifted and unshifted) in sequence.

4. Verify that:

   a. Keys do not stick.

   b. Characters appear on the screen as keys are pressed.

   c. Appropriate character appears on screen for corresponding key (depends upon character set; selectable in Set-up mode).

   d. Only one character appears on the screen when each key is pressed and released once.

5.4 VIDEO ADJUSTMENTS

Seven adjustments on the Video PWBA, as shown in Figure 5-1, permit adjustment of the brightness, focus, vertical size, vertical linearity, and horizontal size. Note that brightness (paragraph 5.4.1) should be adjusted prior to performing the other adjustments.

5.4.1 Brightness

1. Apply power to the terminal. Place the terminal in local mode (enter Set-up mode).

2. Select a reverse video background (Status Line 2 in Set-up mode).

3. Enter a SHIFT/S to generate a reverse video display.

4. Turn the intensity control dial (under lower-right corner of display screen on exterior of case) to maximum intensity (refer to Figure 2-3).

5. Remove the top cover (see paragraph 6.3.1).

6. Adjust brightness (VR301 on Video PWBA: see Figure 5-1) so that CRT display is at maximum brightness but no raster is visible.

7. Using the intensity control dial, lower the CRT brightness to a comfortable viewing level.

8. Remove power from the terminal.

9. Replace the top cover.

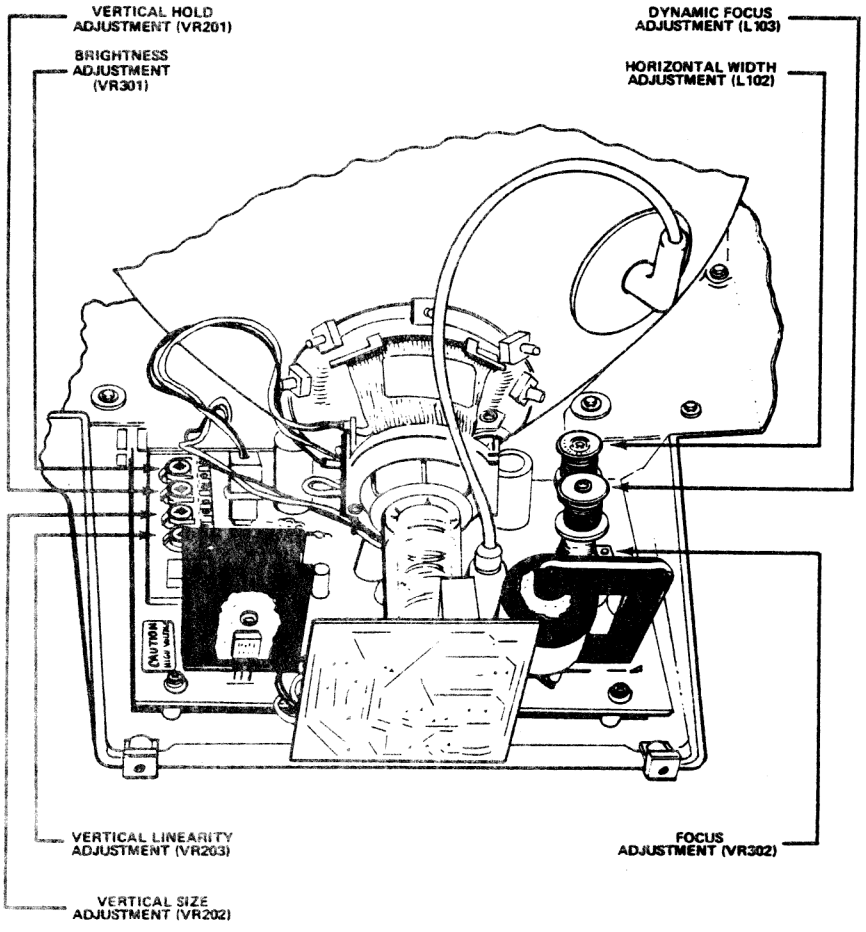


Figure 5-1. Video Adjustments

5.4.2 Focus

1. Apply power to the terminal. Place the terminal in local mode (enter Set-up mode).
2. Fill the screen with exclamation marks (!).
3. Remove the top cover.
4. Adjust Focus (VR302 on Video PWBA for center focus; focus coil L103 for edge focus: see Figure 5-1) so that the dot of every exclamation mark (in both center and edge areas of the screen) is clearly separated.
5. Remove power from the terminal.
6. Replace the top cover.

5.4.3 Vertical Size

1. Apply power to the terminal.
2. Enter Set-up mode and place terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust the vertical dimension of the video display (VR202 on Video PWBA: see Figure 5-1) to 172mm (±3mm).
6. Remove power from the terminal.
7. Replace the top cover.

5.4.4 Horizontal Size

1. Apply power to the terminal.
2. Enter Set-up mode and place the terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust the horizontal dimension of the video display (L102 on Video PWBA: see Figure 5-1) to 239 mm (±5mm).
6. Remove power from the terminal.
7. Replace the top cover.

5.4.5 Vertical Linearity

1. Apply power to the terminal.
2. Enter Set-up mode and place the terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust vertical linearity (VR203 on Video PWBA: see Figure 5-1) so that typical dimensions of any "E" character are within 15 percent of the dimensions illustrated in Figure 5-2.
6. Remove power from the terminal.
7. Replace the top cover.

5.5 TROUBLESHOOTING

Figure 5-3 is an interconnection diagram of the terminal. The waveforms provided in Figures 5-4 through 5-8 are representative of typical oscilloscope CRT displays.

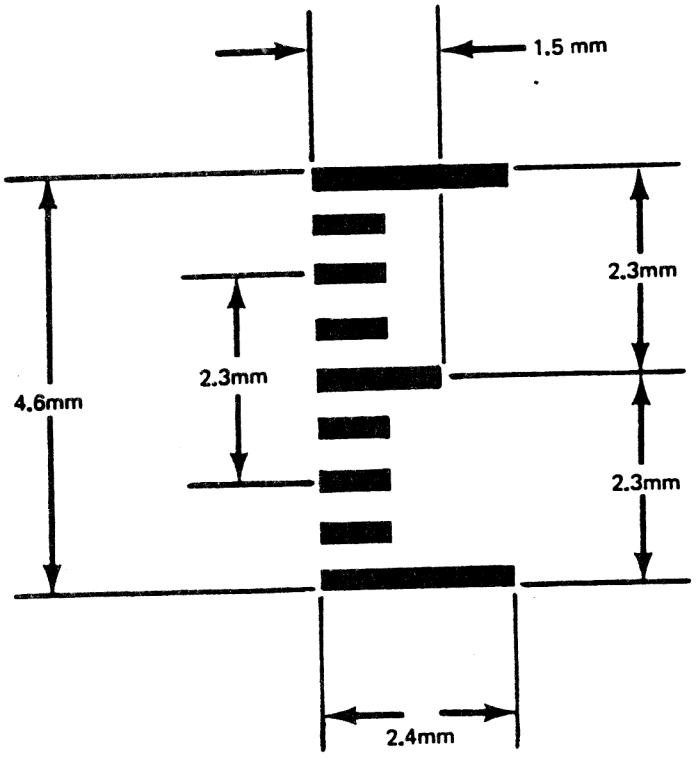


Figure 5-2. Dimensions of E Character

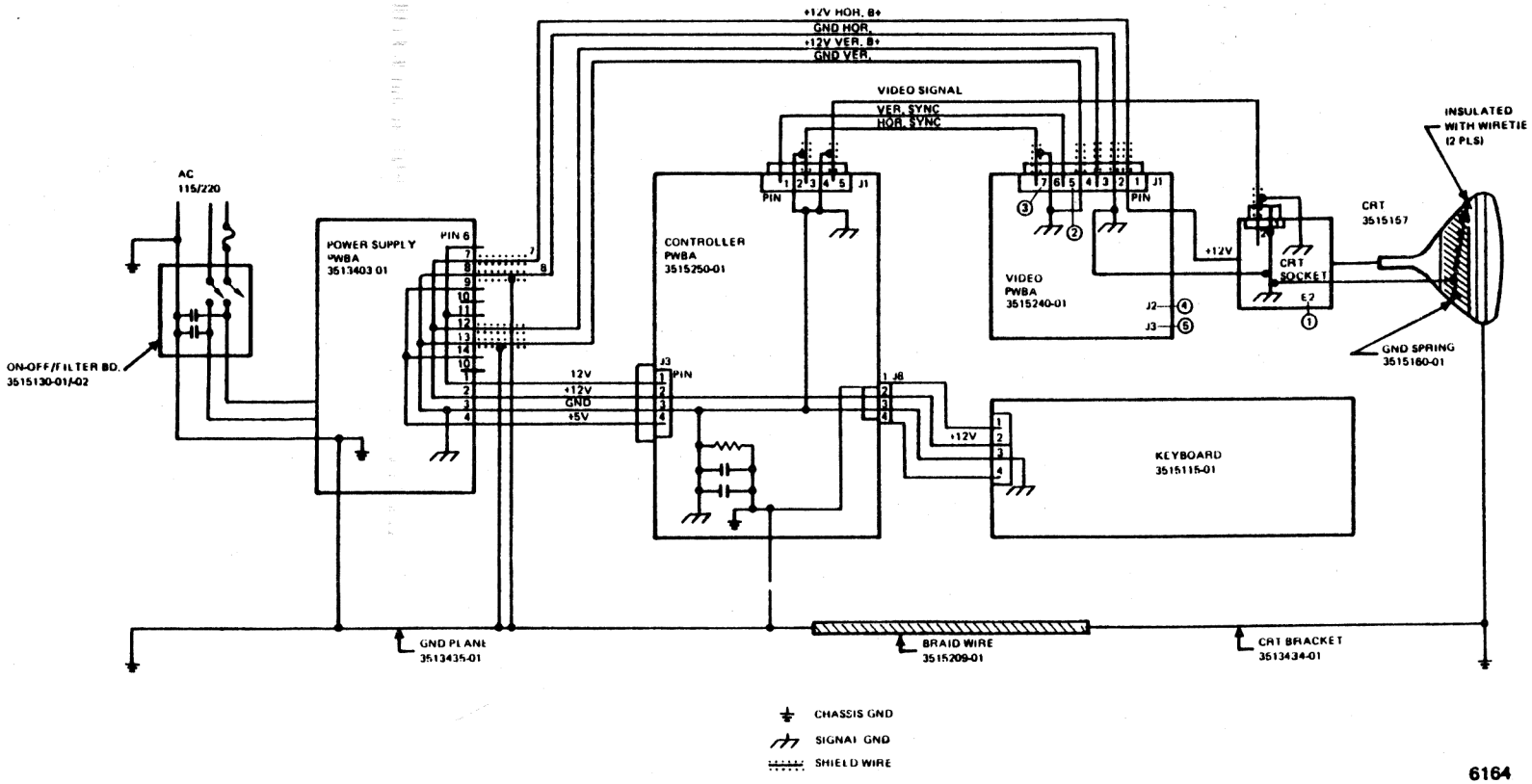


Figure 5-3. Interconnection Diagram

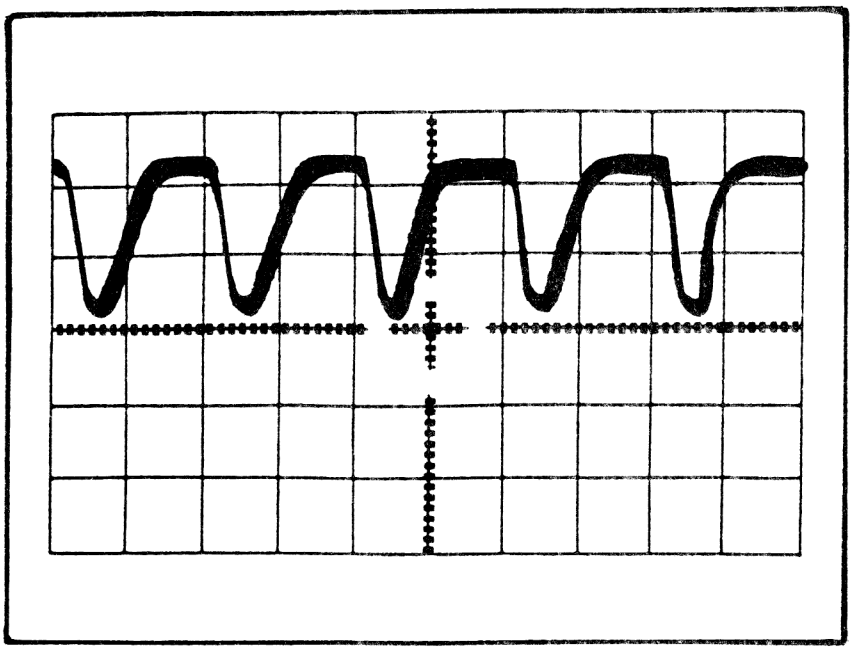


Figure 5-4. Video Waveform

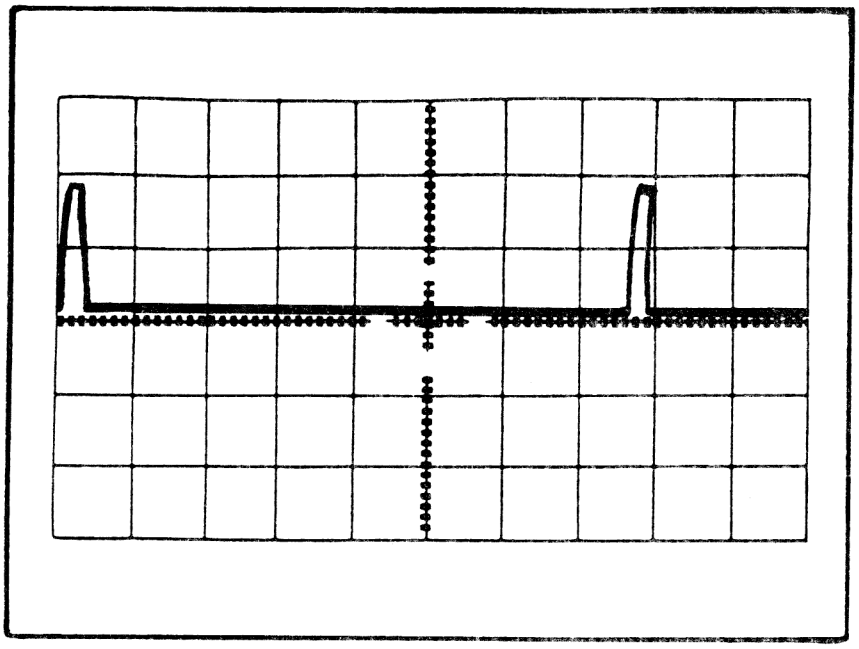
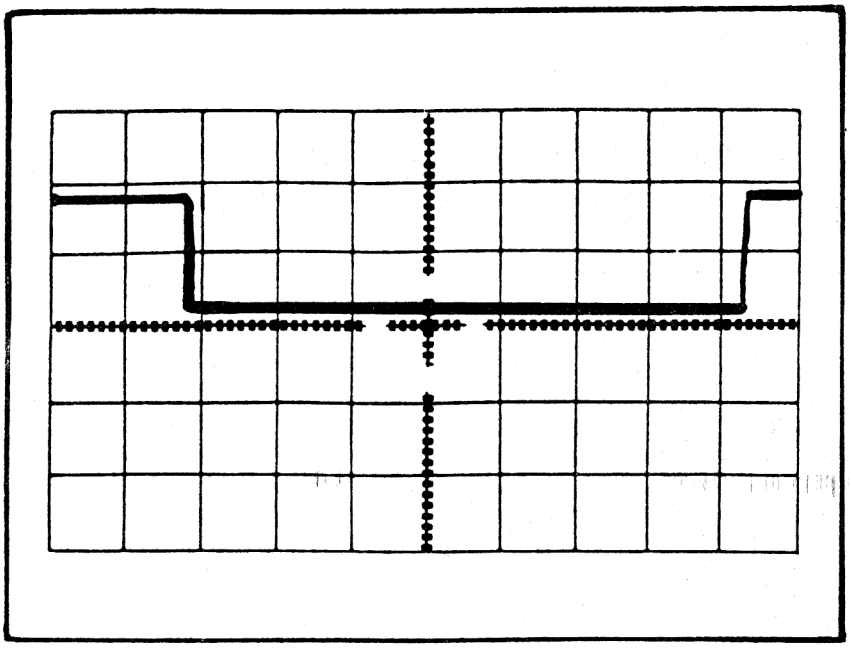


Figure 5-5. Vertical Sync Waveform

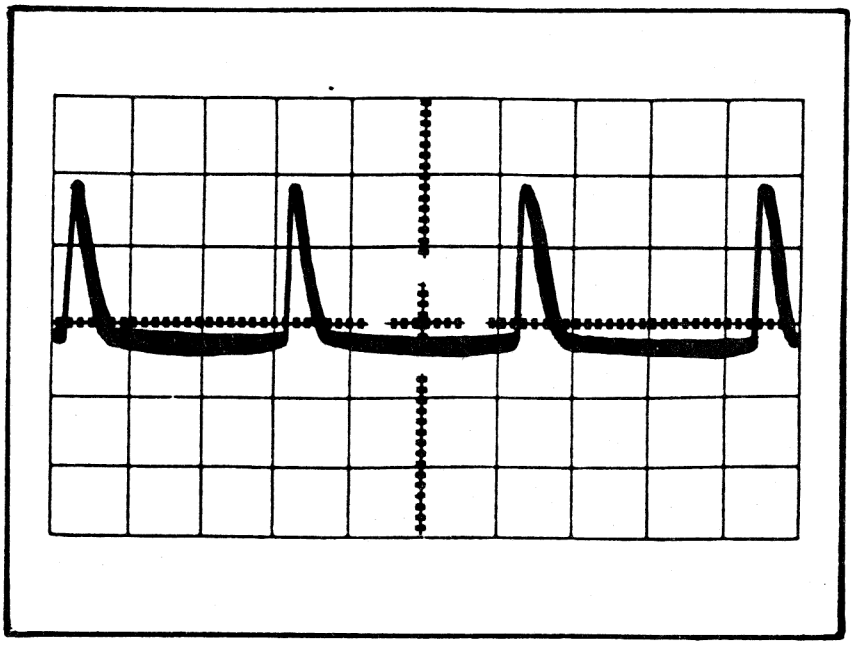


TEST POINT
J1–7–③

2V/DIV @ 5 MICROSECONDS

6203

Figure 5-6. Horizontal Sync Waveform

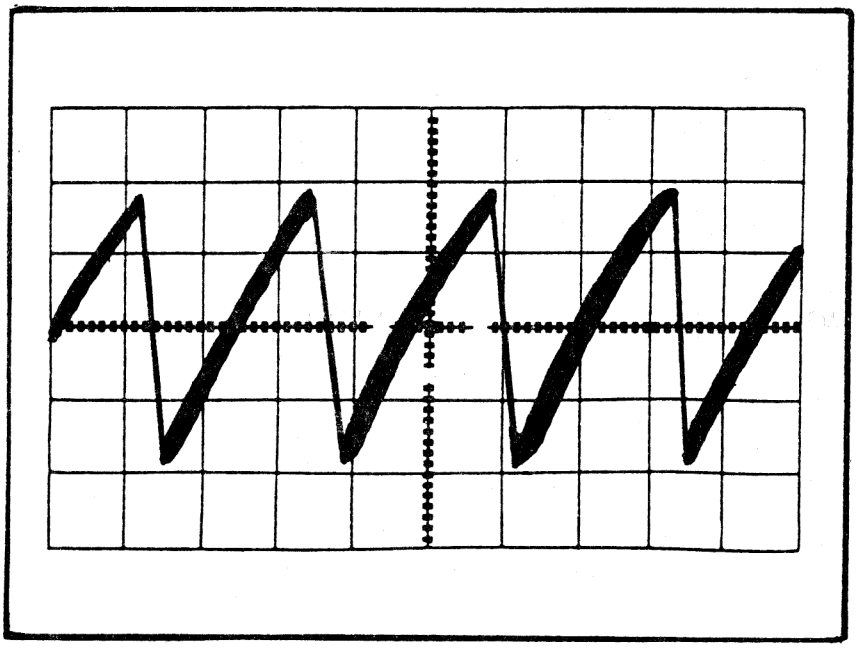


TEST POINT
J2–④

200 MA/DIV @ 5 MILLISECONDS

6204

Figure 5-7. Vertical Deflection Waveform



TEST POINT
J3-5

2A/DIV. @ 20 MICROSECONDS

6205

Figure 5-8. Horizontal Deflection Waveform

SECTION VI
REMOVAL AND REPLACEMENT

6.1 INTRODUCTION

This section provides instructions for the removal and replacement of the Ampex 210's major replaceable parts.

WARNING

There are hazardous voltages inside the pedestal and display units. Extremely high voltages are present on the CRT. The CRT may retain a charge for an indefinite period of time if not discharged. Always discharge the CRT before replacing it or working near it.

6.2 SUBASSEMBLY/PARTS LOCATION

Table 6-1 provides a list of removable parts and subassemblies for the Ampex 210 terminal. Figure 6-1 is an exploded view of the location of those parts and subassemblies.

Table 6-1. Subassembly and Parts List

Ref Fig. 6-1	Subassembly/Part	Part No.
A	Pedestal Assembly	3515150-01
B	CRT Housing, Bottom	3513426-01
	Ground Spring Assembly	3515160-01
C	Video, PWBA	3515240-01
D	CRT Housing, Top	3513427-01
E	Video, PWBA (hard-wired to major board)	3515240-01
F	Pedestal Unit, Top	3513425-01
G	CRT Amber	3515151-03
	CRT Green	3515151-02
	Intensity Control Assembly	3515233-01
H	Yoke/Cable Assembly	3515158-01
I	Controller, PWBA	3515250-01
J	VPA Power Switch	3515130-01
K	Power Supply, PWBA	3513403-01
	Choke Assembly	3515230-01
L	Keyboard Assembly	3515170-01
	Keyboard Cover	3513420-01
	Keyboard Base	3513421-01
	Coil, Cable 6-ft	3515147-01

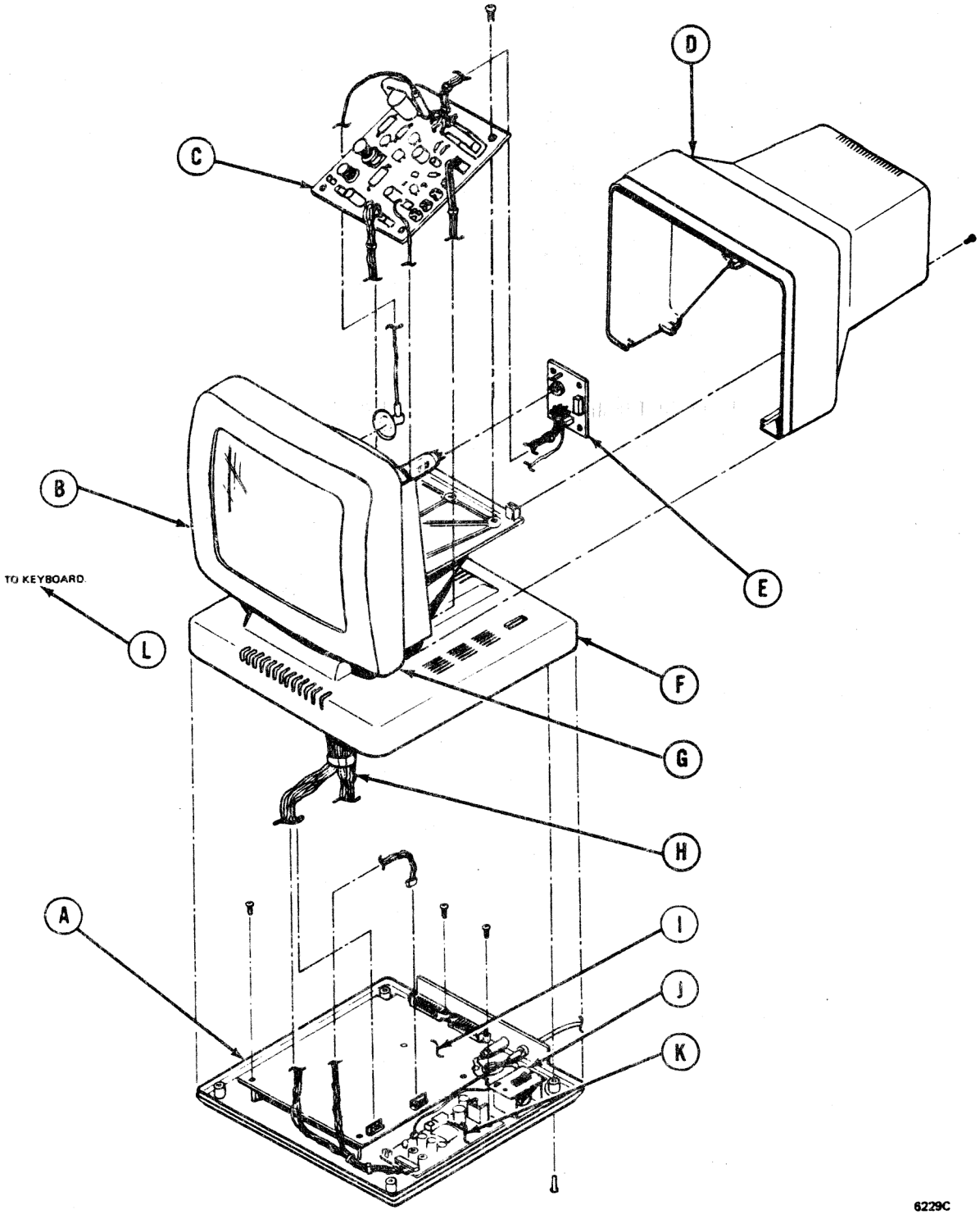


Figure 6-1. Subassembly Location Diagram

6.3 PRELIMINARY PROCEDURE

Before removing or replacing any of the parts of the Ampex 210 terminal, turn the power off and unplug power cord. Disconnect the keyboard cable from the display unit. When removing parts with cable or wire connections, it is recommended that the cables or wires are tagged in order to ensure correct replacement.

6.3.1 Display (Bezel) Cover Removal And Replacement

Using a Phillips screwdriver, remove the two screws at the rear of the display unit. Carefully slide the cover away from the screen (Figure 6-2). When cover will slide no further, gently tilt cover up and lift off.

Replacement is the reverse of removal. Ensure that the sides of the cover slide into place before replacing the two screws at the rear of the cover.

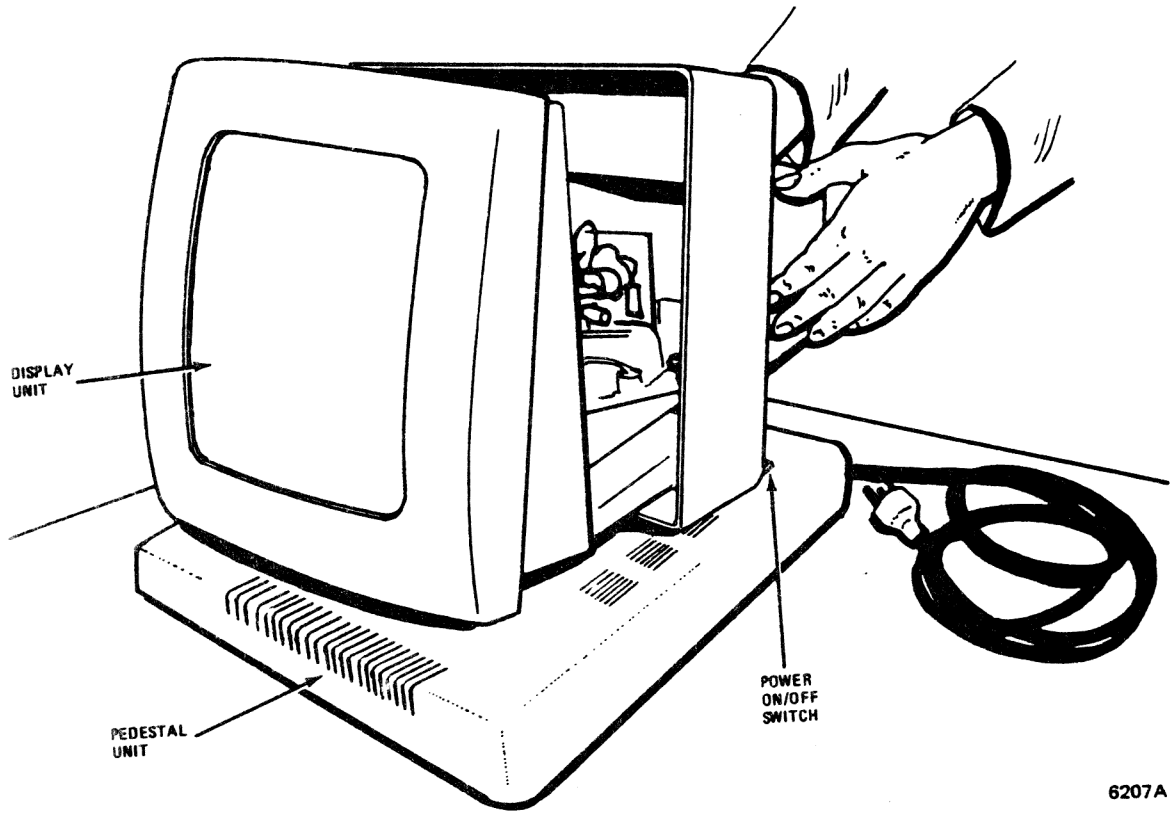


Figure 6-2. Removing the Display Cover

6.3.2 Pedestal Cover Removal And Replacement

Tilt the display assembly until the unit is resting on its side.

Using a Phillips screwdriver, remove the four screws on the underside of the pedestal unit. Gently force the bottom cover away from the display (Figure 6-3).

Replacement is the reversal of removal. Make sure that the bottom cover is in place before replacing the four screws.

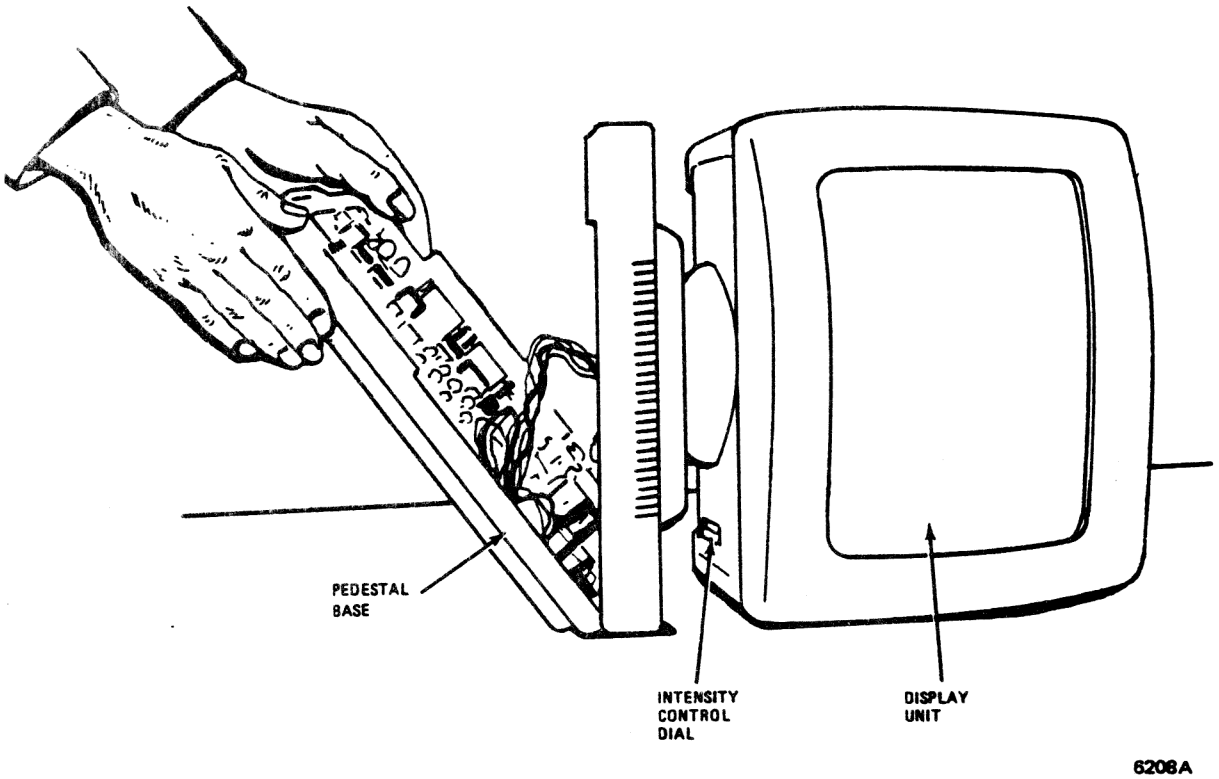


Figure 6-3. Removing the Pedestal Cover

6.3.3 Controller PWBA Removal And Replacement

The Controller printed wiring board assembly (PWBA) is located in the pedestal unit (refer Figure 6-1).

1. Using a Phillips screwdriver, remove the screws holding the board in place.

2. Tag and disconnect any cables connected to the board.

3. Slowly slide the board away from the two RS232C serial ports. When the serial connectors are free of their ports, lift the board up and out of the unit.

To replace the board, reverse the procedure. Make sure the board is firmly seated before replacing the screws.

6.3.4 Power Supply PWBA Removal And Replacement

The power supply PWBA is located in the pedestal unit (see Figure 6-1).

1. Using a Phillips screwdriver, remove the four screws holding the power supply board in place.

2. Tag and disconnect any cables connected to the board.

3. Slowly pull the board up and out of the pedestal unit.

To replace the power supply board, reverse the procedure. Make sure the board is firmly seated before replacing the screws.

6.3.5 Discharging The CRT

WARNING

The CRT Anode may stay charged at an extremely high voltage for a long time after the power is removed from the terminal. Be sure to follow the CRT discharging procedure carefully. Make sure that a good discharge path is made between the ground wire around the CRT and anode connector beneath rubber cover.

1. Make sure that power is off and that the power cord is disconnected from the ac power outlet.

2. Using a wire lead with an alligator clip on each end, connect one alligator clip to ground screw and the other clip to a flat-blade screwdriver with an insulated, rubber handle (Figure 6-4).

3. Hold the screwdriver by the insulated handle with one hand and move the other hand away from the unit.

4. Slip the screwdriver blade under the rubber anode cover and touch the end of the anode lead. This action should discharge the CRT through the ground wire.

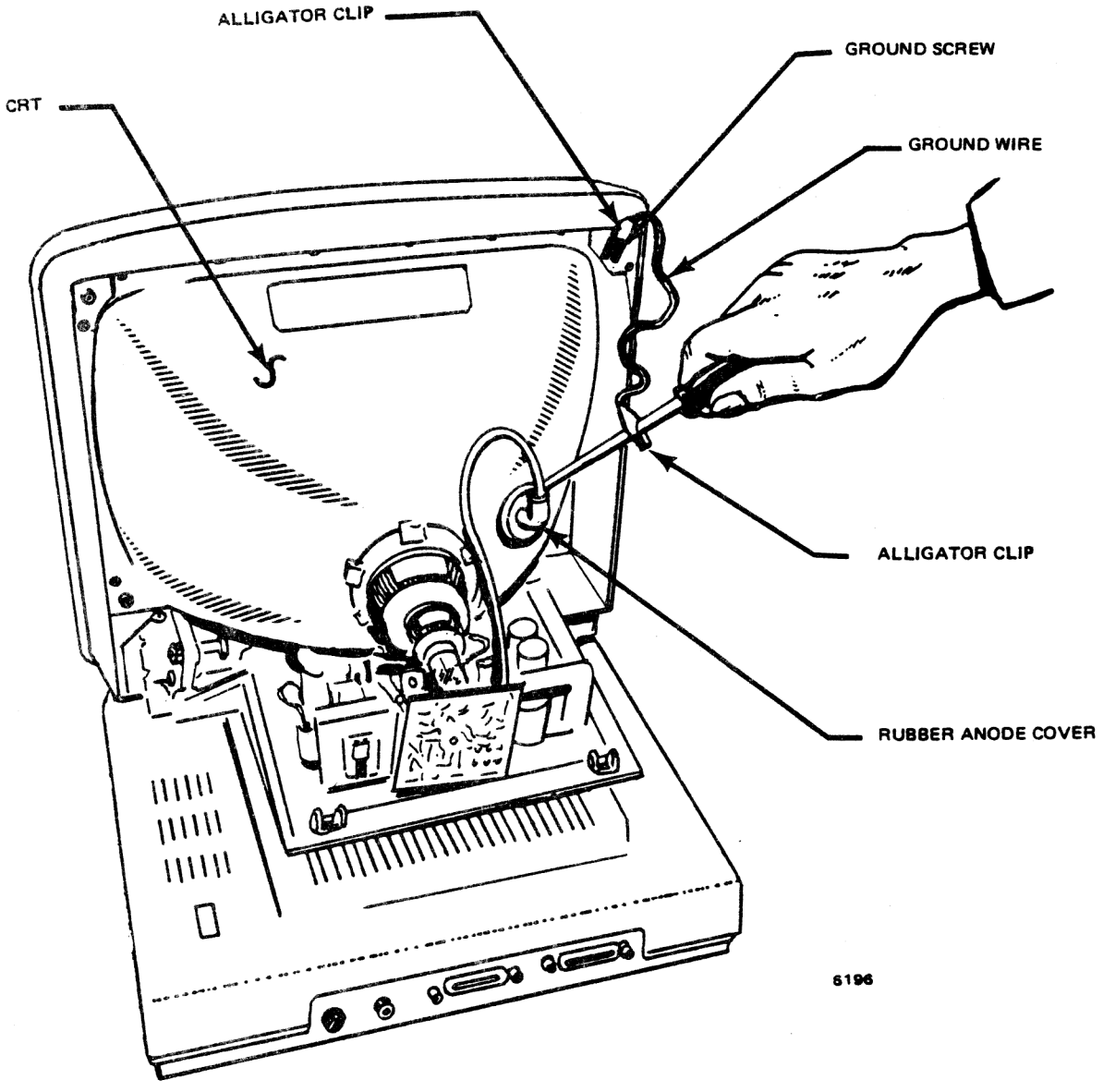


Figure 6-4. Discharging the CRT

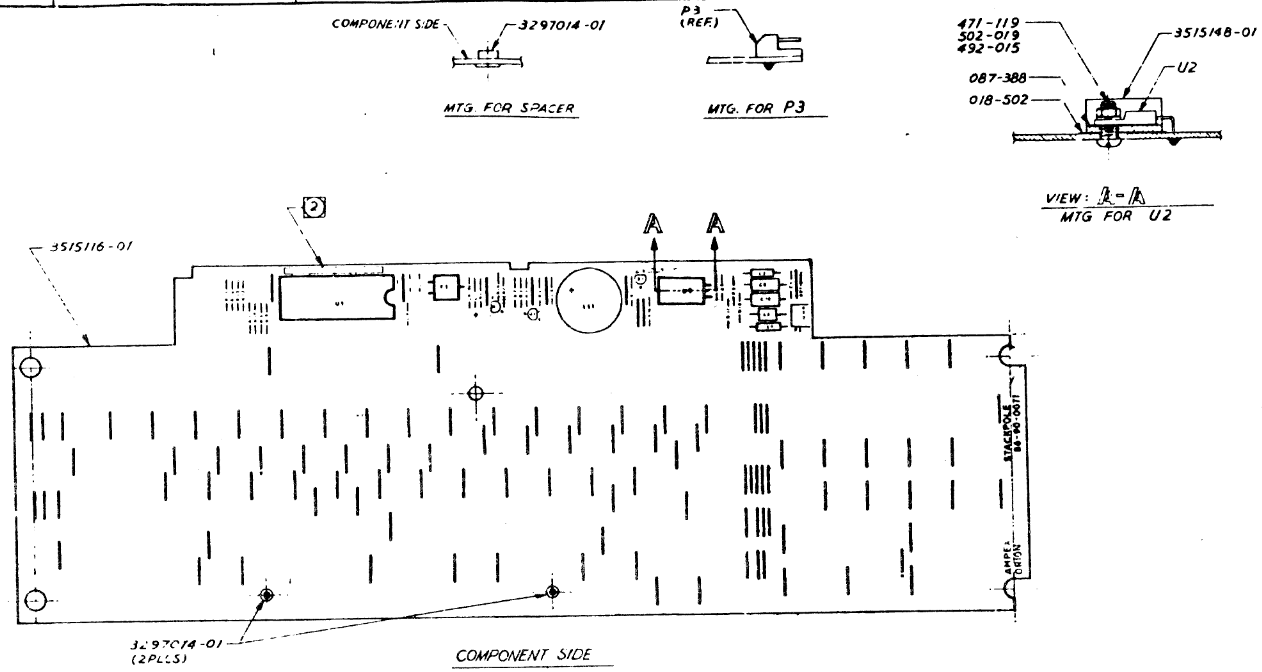
6.3.6 Video PWBA Removal and Replacement

The video PWBA (board) is located in the display (bezel) unit (see Figure 6-1). Make sure the CRT has been discharged before removing the video board.

1. Pull up on the two black plugs in the corners of the video board until they pop out.
2. Tag and disconnect any cables attached to the board.
3. Gently slide board away from the screen. Then lift up and remove from the bottom of the unit.

To replace the board, reverse the procedure. Make sure the board is firmly seated before replacing the cover of the display unit.

LTR	ZONE	REVISIONS DESCRIPTION	DFTG	CHK	ENGRG
S		[illegible] 4 [illegible]			
G		ERN 0024 (CONT.)			
H		ECN 42031			
J		ECN 42039			



REFERENCE DESIGNATION TABLE

ITEM	PART. NO	DESCRIPTION		REMARK
1	3515116-01	PWB KEYBOARD		
2	517-435	U2	VOLTAGE REGULATOR	IC 7805
3	580-647	Q1, Q2	TRANSISTOR	2N 3904
4	580-800	Q3	TRANSISTOR	2N 5550
5	017-238	Y1	CRYSTAL	4.3152 MHz
6	550 333	LS1	BUZZER	PIEZOELECTRIC
7	066-668	R1, R3, R6,	RESISTOR	4.7KΩ, 1/4W, ±5%
8	066-830	R2, R8, R17, R19	"	10KΩ, 1/4W, ±5%
9	066-664	R4, R7	"	510Ω, 1/4W, ±5%
10	066-677	R5	"	68Ω, 1/4W, ±5%
11	066 839	R18	"	560Ω, 1/4W, ±5%
12				
13	063-460	C10	CAP. LYTIC	47u, 16V, +75 -10 %
14	064-937	C1, C2	CAP. DISK ALTERNATE 064-460	22P, 50V, ±5%
15	3512836-01	C4, C5	CAP. MONO	330P, 50V, ±5%
16	063 456	C3	CAP. LYTIC	1u, 50V, +75 -10 %
17	063 458	C6	CAP. LYTIC	10u, 35V, +75 -10 %
18	064 341	C7-C9	CAP. MONO ALTERNATE 064-458	0.1u, 50V.
19				
20	581-105	CR1, CR2	DIODE, SWITCHING ALTERNATE 581-433	1N4148

ITEM	PART NO	DESCRIPTION		REMARK
21	068-303	L2	CHOKE	33uH, 200MA, ±10%
22	068-304	L1	CHOKE	22uH, 190MA, ±10%
23	068-305	L3	CHOKE	25uH, 200MA, ±10%
24				
25	615-012	WIRE,	SOLID BARE	AWG. #20
26	135-549	P3	RT ANGLE HEADER	4 PIN
27	582-203	XU1	SOCKET	40 PIN
28				
29				
30	3515148-01	HEAT SINK		
31	3297014-01	SPACER		
32				
33				
34				
35				
36				
37				
38				
39				
40				

7. MAX. LEAD PROTRUSION OF COMPONENTS ON SOLDER SIDE IS 1.6 MM.
6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.
5. COMPONENT MUST NOT EXTEND BEYOND OUTLINE OF BD.
4. ASSEMBLE PER AMPEX STD.
3. FOR LOGIC DIAGRAM SEE SH 2.
[2] MARK ISSUE LTR. AND SERIAL NO. PER AMPEX SPEC 3124500 PARA 3.1.
1. PART NO. TO BE 3515115-01.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
	ORION
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL: 2 PL, 3 PL, ANGLE
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AMD 10,127
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

DRAWN BY / CHK BY / DFTG APVD / ENGRG APVD / AUTH BY

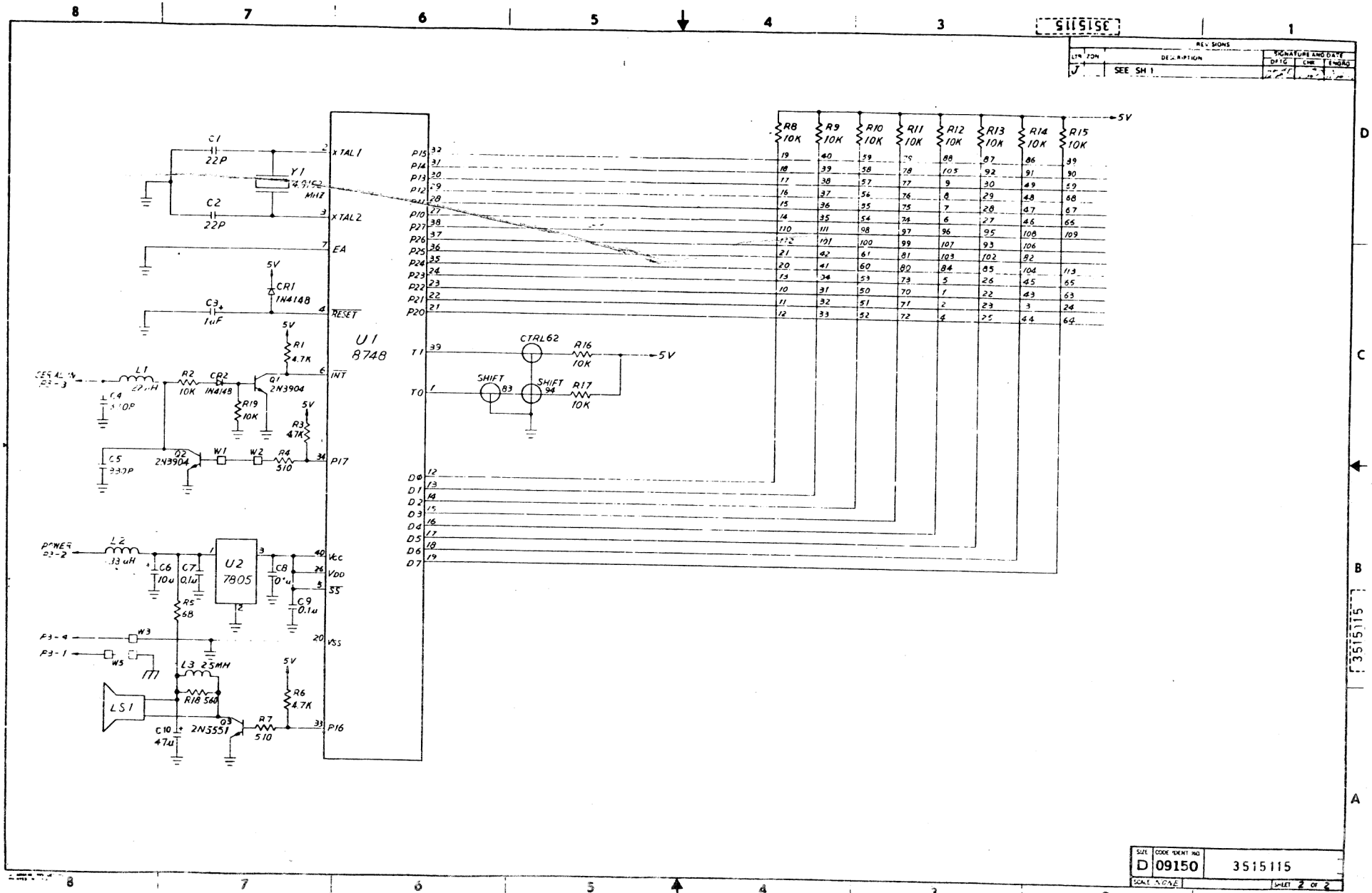
AMPEX — MEMORY PRODUCTS DIVISION

PWBA-KEYBOARD

SIZE D | CODE IDENT NO 09150 | 3515115

SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 2

[3515115]



REVISIONS			
LTR	ZON	DESCRIPTION	SIGNATURE AND DATE
J		SEE SH 1	

SIZE	CODE IDENT NO	
D	09150	3515115
SCALE NONE		SHEET 2 OF 2

3515115

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		SEE SH. 1	—	—	—

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARKS	Q'TY
1	3515141-01		HEATSINK HOR/VER.	1
2	3515142-01	T101	X'FORMER HOR. OUTPUT	1
3	3515143-01	L103	COIL, FOCUS	1
4	3505211-01	L102	COIL, HOR. WIDTH	1
5	3505212-02	L101	COIL, HOR. LINEARITY	1
6				
7	581-687	CR301	1N4003	1
8	013-871	CR302, CR303	1N4006	2
9	581-725	CR103	MR852/GI852	1
10	581-485	CR102	MR854/GI854	1
11	581-403	CR101	SWITCHING	1
12				
13	579-048	Q101	MPS 9434J	1
14	580-647	Q402	2N3904	1
15	579-151	Q401	2N6553	1
16	579-154	Q102	BU806	1
17				
18	002-036	U201	μPC1031H2/LA1385	1
19				
20	075-364	VR203	2KΩ	1
21	075-365	VR202	20KΩ	1
22	075-366	VR201	50KΩ	1
23	075-367	VR301	500KΩ	1
24	075-376	VR302	2MΩ, X-201-RS	1
25				
26	066-834	R407, R103	33Ω, 5%, 1/4W	2
27	066-938	R411, R406	47Ω, " , "	2
28				
29	066-835	R207	82Ω, " , "	1
30	066-663	R402	220Ω, " , "	1
31	066-814	R301	270Ω, " , "	1
32	066-665	R101, R208, R403	1KΩ, " , "	3
33	066-675	R404	1.8KΩ, " , "	1
34	066-666	R203	2.7KΩ, " , "	1
35	066-829	R201, R204, R205	6.8KΩ, " , "	3
36	066-847	R202	33KΩ, " , "	1
37	066-913	R302, R304, R305	220KΩ, " , "	3
38	066-673	R303	1MΩ, " , "	1
39	062-182	R408	1KΩ, " , 1/2W	1
40	062-199	R410, R409	10KΩ, " , 1/2W	2
41	079-425	R206	1Ω, " , 1W	1
42	079-427	R102	100Ω, " , 2W	1
43	059-885	R401	820Ω, " , 4W	1
44	066-560	R306	56Ω, " , 1/4W	1
45	066-838	R405	330Ω, " , 1/4W	1

ITEM	PART NO.	DESCRIPTION	REMARKS	Q'TY
46	064-993	C402	120PF, 50V, ±5%	1
47	064-975	C107, C401	0.1μF, 50V, +80 -20 %	2
48	030-299	C106	0.001μF, 1KV, 20%	1
49	030-129	C105, C304, C305, C404	0.01μF, 1KV, 20%	4
50	064-410	C212, C209, C205	0.047μF, 50V, 20%	3
51	064-133	C303, C306	0.33μF, 100V, 20%	2
52	3512840-02	C102	0.027μF, 400V, 5%	1
53	037-493	C202	1μF, 15V, 20%	1
54	067-116	C210, C211	22μF, 10V, 10%	2
55	063-459	C101, C201, C204	10μF, 16V, 20%	3
56	063-552	C207	100μF, 10V, 10%	1
57	063-460	C206	47μF, 16V, +50 -10 %	1
58	063-461	C108, C203	220μF, 16V, +75 -10 %	2
59	063-462	C208	2200μF, 16V, +75 -10 %	1
60	063-553	C104	100μF, 25V, +75 -10 %	1
61	063-554	C302	100μF, 80V, +75 -10 %	1
62	063-551	C301, C403	10μF, 100V, +75 -10 %	2
63	3505539-01	C103	25μF, 25V, 20%	1
64				
65				
66	064-984	SG401, SG402, SG403	SPARK-GAP, 1KV, GAP-R75	3
67				
68	060-049	NS401	NEON LIGHT, 105VAC, 2mA	1
69	012-270	S401	SOCKET, 7P, CRT BASE	1
70				
71	135-534	J1	HEADER, 7-P	1
72	135-530	J2, J3, J5	HEADER, 2-P	3
73	135-531	J4	HEADER, 3-P	1
74				
75	177-352	GND.	PIN DISCONNECT	1
76	615-012	W301	WIRE, SOLID, BARE #20	1
77				
78				
79				
80				
81				
82				
83				
84				
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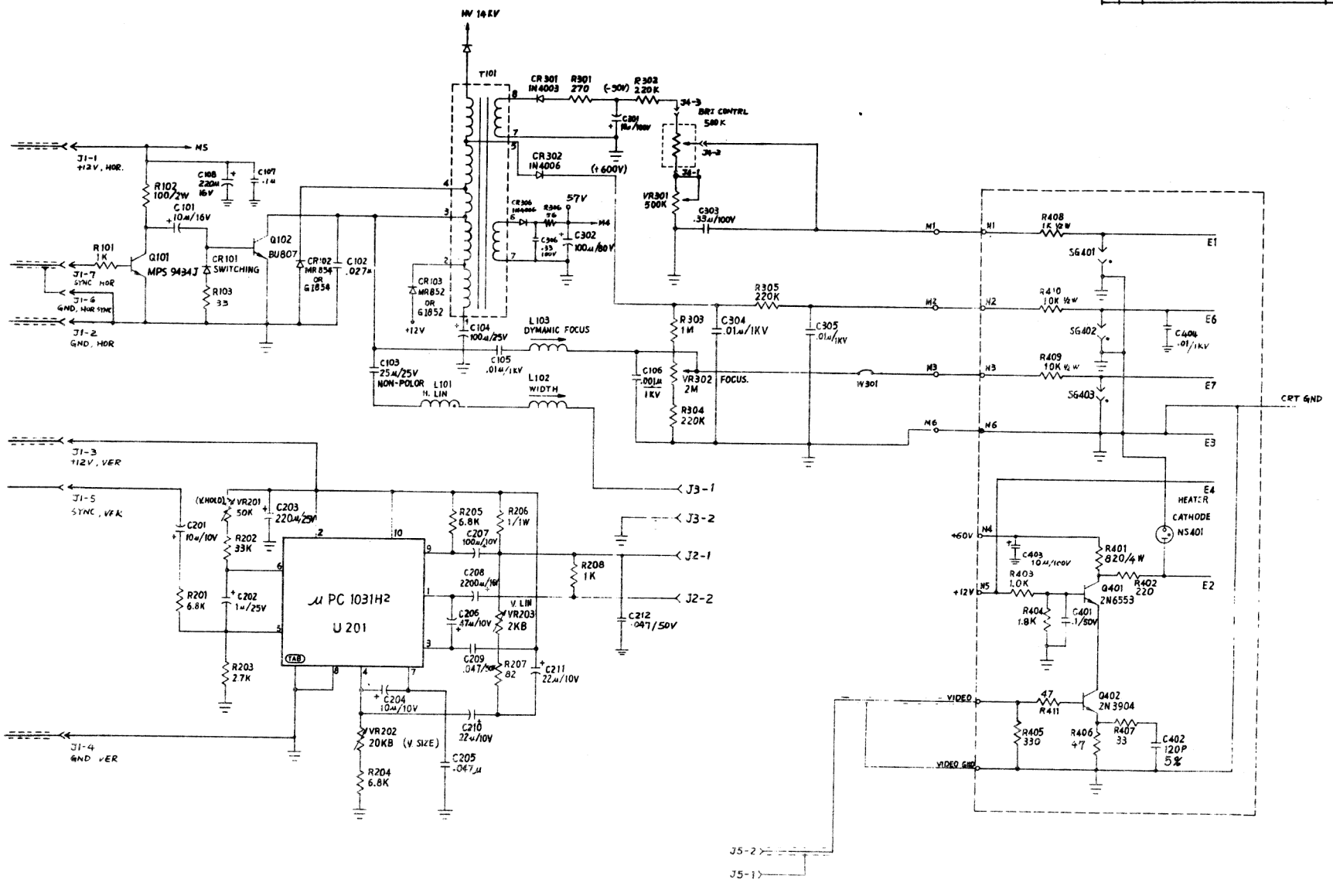
89				
90				

3515240

SIZE	CODE IDENT NO.	
D	09150	3515240
SCALE		SHEET 2 OF 4



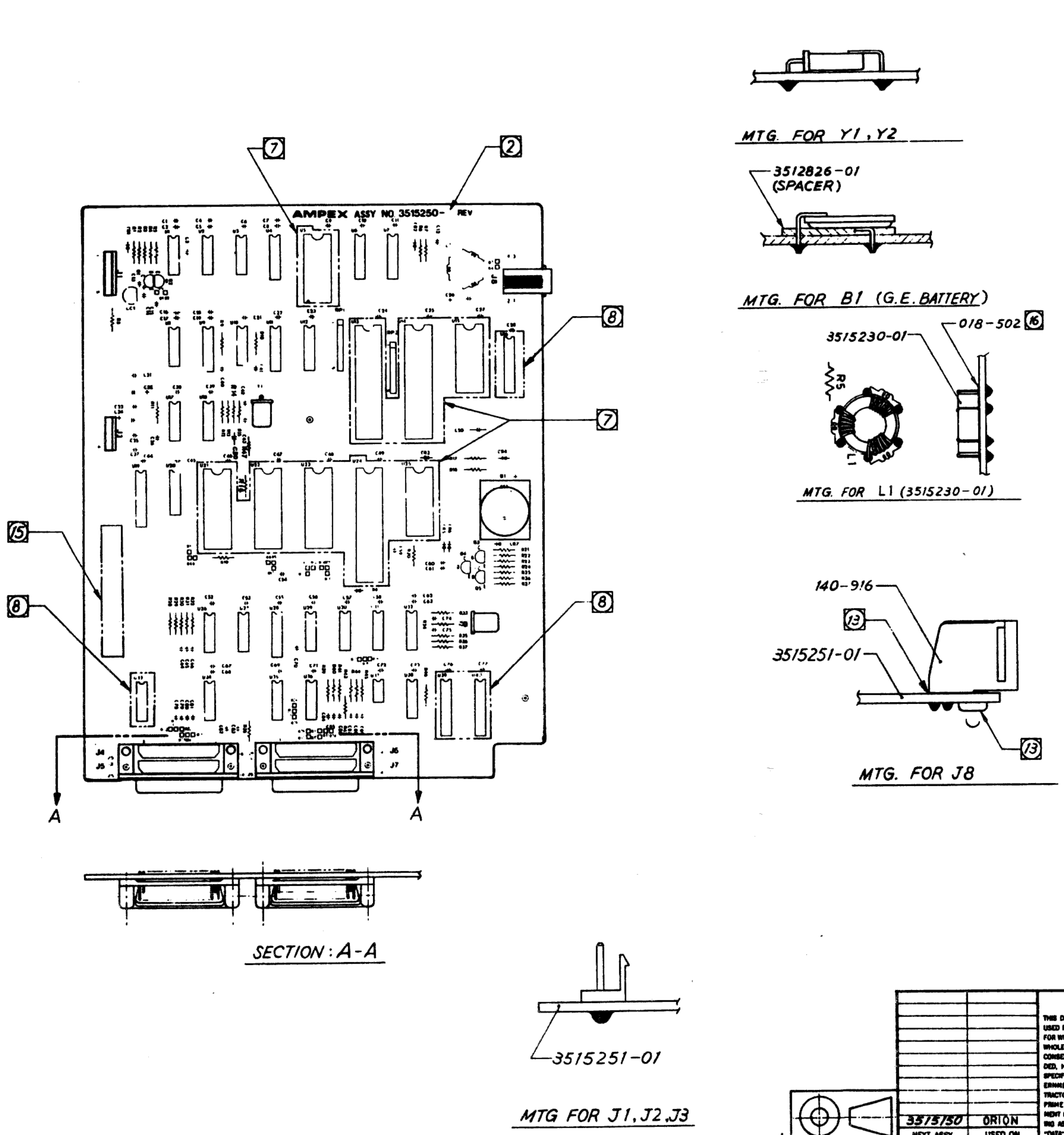
SIZE	CODE IDENT NO.	
D	09150	3515240

SCALE NONE SHEET 3 OF 5

3515250

REVISIONS

LTR	ZONE	DESCRIPTION	DFTG	CHK	ENGRG
A		NEVER RELEASE	—	—	—
B		NEVER RELEASE	—	—	—
C	☆	ERN 0024 (CONT.)			
D		ECN 42027			
E		ECN 42042			



17 FOR REWORK INSTRUCTIONS TO PWBA'S USING "A" ISSUE A/W. SEE ECN 42027.

[16] ASSEMBLE PER AMPEX STANDARD HC 2-17.

[15] ADHERE MASR LABEL TO THIS AREA AFTER MARKING P/N & REV. LETTER.

~~14 SOLDER GROUND LUG (3515239-01) ON THE MTG HOLE OF J4.~~

[13] HEAT SEAL 2 PLASTIC INTERLOCKER OF J8 TO CONSOLIDATE J8 TO BOARD. OR BOND IT TO BOARD WITH 018-502 ADHESIVE.

12 OBSERVE "STATIC CHARGE" PRECAUTIONS WHEN HANDLING SEMICONDUCTOR DEVICES.

~~11 FOR CURRENT LOOP USE ONLY.~~

10 RP1-1 SHOULD BE ORIENTED ON TOP SIDE.

~~9 PULL UP RESISTORS ARE 4.7K OHMS.~~

[8] UNUSED IC POSITIONS: U16, U33, U39, U40. ARE TO BE KEPT FREE OF SOLDER.

[7] FOR INSTALLATION OF EPROM OR ROMS AT: U5, U22, U23. SEE VERSION TABLE. (SH.2) SOCKETS ARE PROVIDED AT (U5, U13, U14, U15, U21, U22, U23, U24, U25).

6 MAX. LEAD PROTRUSION ON SOLDER SIDE IS 2.3 mm.

5 ASSEMBLE PER AMPEX STANDARDS.

4 COMPONENT DESIGNATION ARE FOR REF. ONLY.

3 FOR SCHEMATICES SEE SHEET 3 THRU 6.

[2] MARK DASH NO. SERIAL NO. AND ISSUE LETTER PER AMPEX SPEC. 3124500 PARA 3.1.

1 PART NO TO BE 3515250-01.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST ☒

NEXT ASSY	USED ON
3515150	ORION

APPLICATION

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

TOL	2 PL	3 PL	ANLR
±	—	—	—

REMOVE BURRS AND SHARP EDGES. DRILL TOL PER AND 10387. INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

SIGNATURE		DATE
DRAWN BY	[signature]	2-10-84
CHK BY	[signature]	2-10-84
DFTG APVD	[signature]	2-14-84
ENGRG APVD	[signature]	2-16-84
AUTH BY	[signature]	2-16-84

AMPEX MEMORY PRODUCTS DIVISION, 200 N. Nash Street, El Segundo, California 90245

PWBA-TERMINAL CONTROLLER ORION I

SIZE	CODE IDENT NO.	
D	09150	3515250

SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 6

3515250

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
E		SEE SH.1			

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARKS
1	3515251-01	PWB TERMINAL CONTROL BOARD	
2			
3	587-410	U28	74 LS 139N
4	587-534	U3	74 LS 08
5	587-523	U27, U29, U35	74 LS 32
6	589-619	U24	Z80A CPU
7	3515261-01	U5 ALTERNATE 3515136-02	CHAR GENERATOR
8	003-027	U21	UART R6551 AP
9	001-983	U14	SCN 2672 AC3N40
10	590-983	U15	TMM 2016P TOSHIBA
11	587-773	U9	74 LS 163
12	587-510	U17	74 LS 00
13	589-449	U19	74 LS 244
14	587-533	U10, U18, U30, U32	74 LS 04
15	PART "A"	U23	SYSTEM ROM 1
16	PART "B"	U22	SYSTEM ROM 2
17	590-108	U34	75188
18	587-856	U26, U36	75189
19	001-908	U25 (CMOS RAM 300 ns)	TC 5517 APL
20	587-291	U37	NE 555
21	587-095	U8	74 S 74
22	587-387	U31, U38	74 LS 74
23	586-325	U1	7405
24	587-746	U2	74 LS 86 N
25	587-770	U6, U7, U11, U12, U20	74 LS 174
26	590-062	U4	74 LS 166
27	3515260-01	U13 ALTERNATE 3515135-01	CRT CONT. I.C.
28			
29			
30			
31			
32	066-668	R6, R9, R19, R20, R31, R32, R37, R40, R41, R46	4.7K OHM, 1/4W, 5%
33	066-821	R33, R34	820 " " "
34	066-849	R42, R43	100K " " "
35	066-838	R4, R17, R35, R36, R3, R15, R47	330 " " "
36	066-830	R38	10K " " "
37	066-665	R13, R18, R21, R24, R27, R2	1K " " "
38	066-689	R22, R45	2.2K " " "
39	066-820	R26	750 " " "
40	076-004	R23	180 " " "
41	066-715	R10	1.2K " " "
42	066-673	R44	1M " " "
43	066-675	R25	1.8K " " "
44	066-834	R16	33 " " "
45	066-812	R8	100 " " "
46			
47			
48	3512803-01	RP1, RP2 RES NETW	SIP 8 RES 22KΩ
49			
50			

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARKS
51	064-997	C1, C4, C12, C16, C18, C36, C64, C65, C66, C70, C78 CERAMIC DISC	330PF, 50V ±10%
52	" "	C79, C80, C81, C84, C85, C86	" " "
53	064-939	C74 CERAMIC DISK ALTERNATE 026-027	.001μF, 50V 2%
54	064-444	C35, C49, C82, C83 CERAMIC MONO	.1μF, 50V +80 -20%
55	064-116	C2, C5, C6, C7, C11, C17, C19, C21, C22, C23, C27, C38, C39	.01μF, 50V 20%
56	" "	C44, C52, C55, C57, C58, C60, C61, C63, C67, C68, C71	" " "
57	" "	, C73	" " "
58	063-391	C32, C34	100μF, 16V
59	064-941	C9, C24, C25, C46~C48, C87~C89, C15 ALTERNATE 064-458	0.1μF, 50V
60	063-461	C26 LYTIC	220μF, 16V -10 +75%
61	064-464	C43,	100PF, 100V ±5%
62	064-937	C42, C75, C30	22PF, 50V
63	064-998	C54	2000PF, 50V ±20%
64			
65			
66	579-156	Q1 XSTR	2SC 1730
67	014-889	Q4, Q5 XSTR	2N 3643
68	014-772	Q3 XSTR	2N 3644
69	581-403	CR1~CR6, CR8	1N 4531
70			
71	582-203	XU13, XU14, XU24 I.C. SOCKET	40 PIN ALTERNATE (582-387)
72	582-202	XU21, XU22, XU23. " "	28 " (582-386)
73			
74			
75			
76	3515139-01	Y2 CRYSTAL	3.6864 MHZ.
77	3515140-01	Y1 CRYSTAL	20.92 MHZ.
78	080-060	B1 LITHIUM	GE 3.0V
79	3512826-01	BATTERY SPACER	
80			
81	135-532	J3 CONNECTOR	4 PIN
82			
83	140-900	J4, J6 "	25 " RS232
84	135-533	J1 "	5 "
85	140-916	J8 KEYBD "	4 "
86			
87			
88	3511043-01	LABEL MASR	
89	3515230-01	L1 CHOKE ASSY	
90			
91	052-036	LC1	EMI FILTER
92			
93			
94			
95			
96			
97			
98			
99			
100			

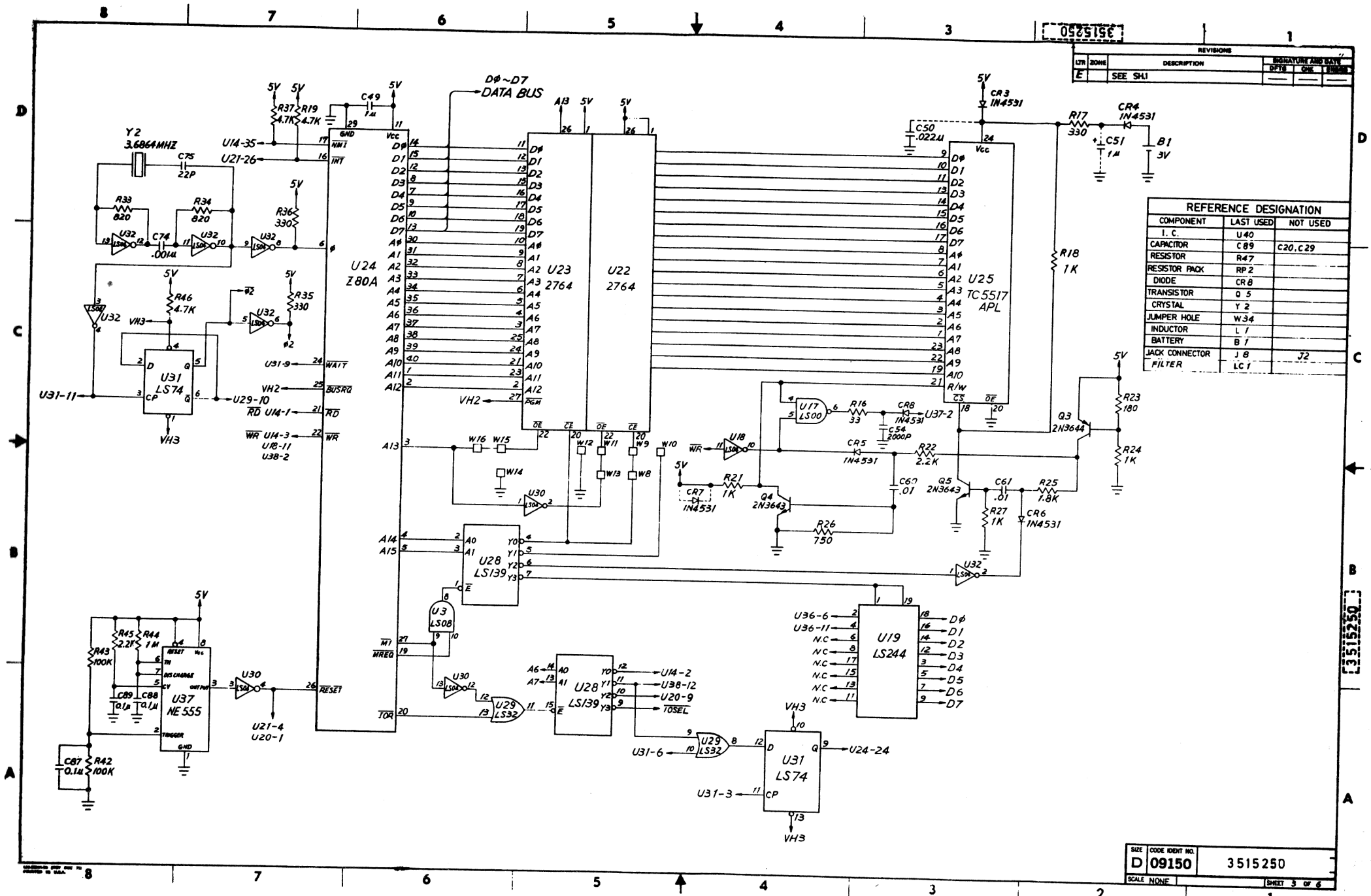
PART NO.	COMPONENTS
3515250-01	INSTALL ALL COMPONENTS SHOWN IN REFERENCE DESIGNATION TABLE EXCEPT : C3, C8, C10, C14, , C28, C31, C33, C37, C40, C41, C45, C50, C51 C53, C56, C59, C62, C69, C76, C77, C13, C72. R1, R5, R7, , R11, R12, R14, R28, R29, R30, R39. U16, U33, U39, U40. J5, J7. CR7. Q2
3515250-02	C3, C8, C10, C14, C28, C31, C33, C37, C40, C41, C45, C50, C51, C53, C56, C59, C62, C69, C76, C77, C13, C72. R1, R5, R7, R11, R12, R14, R28, R29, R30, R39. U16, U22, U33, U39, U40, XU22 J5, J7. CR7. Q2

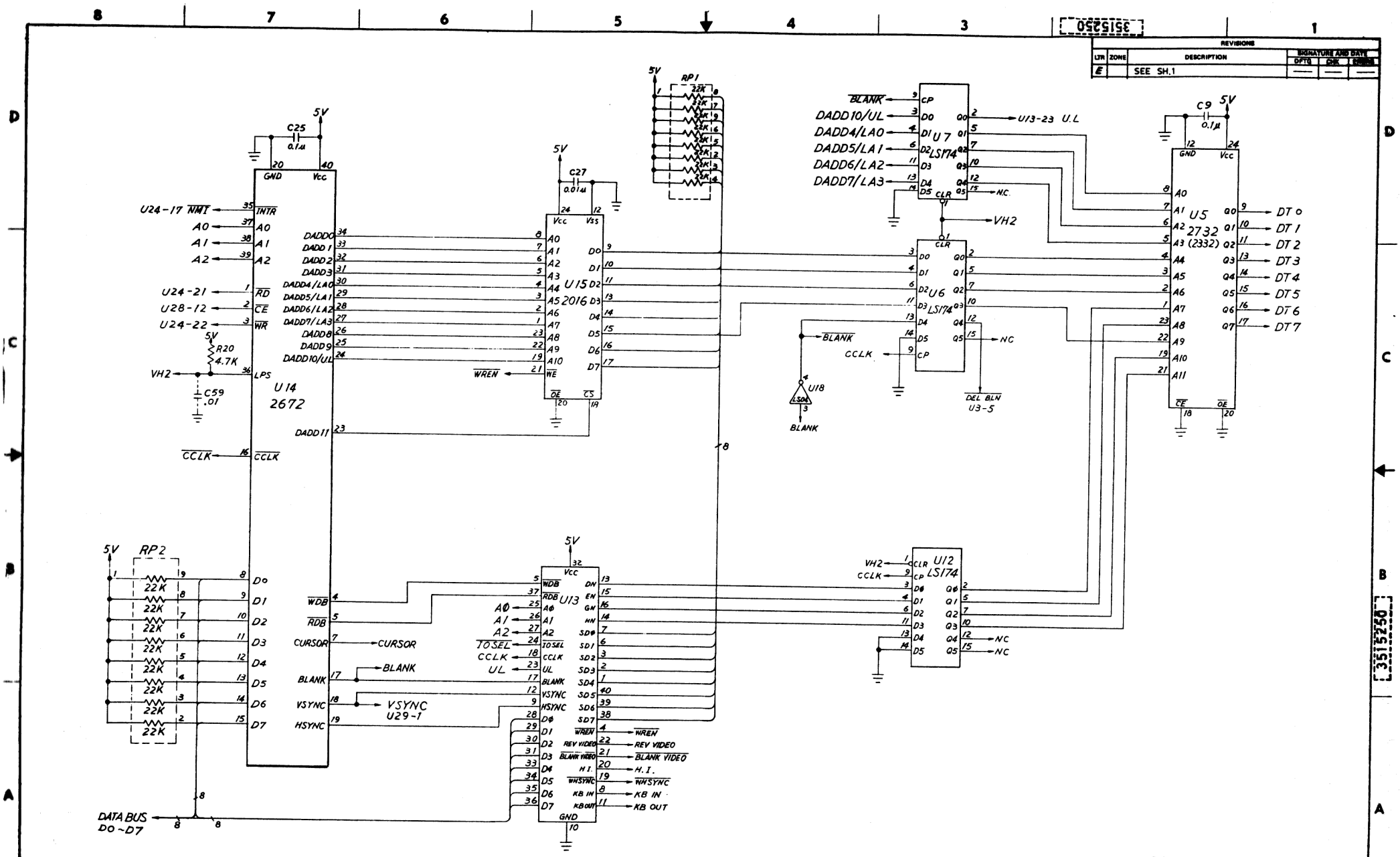
3515250-02	3515264-01	—
3515250-01	3515262-01 ALTERNATE 3515137-02	3515263-01 ALTERNATE 3515139-02
PART NO.	PART "A"	PART "B"
	VERSION TABLE	

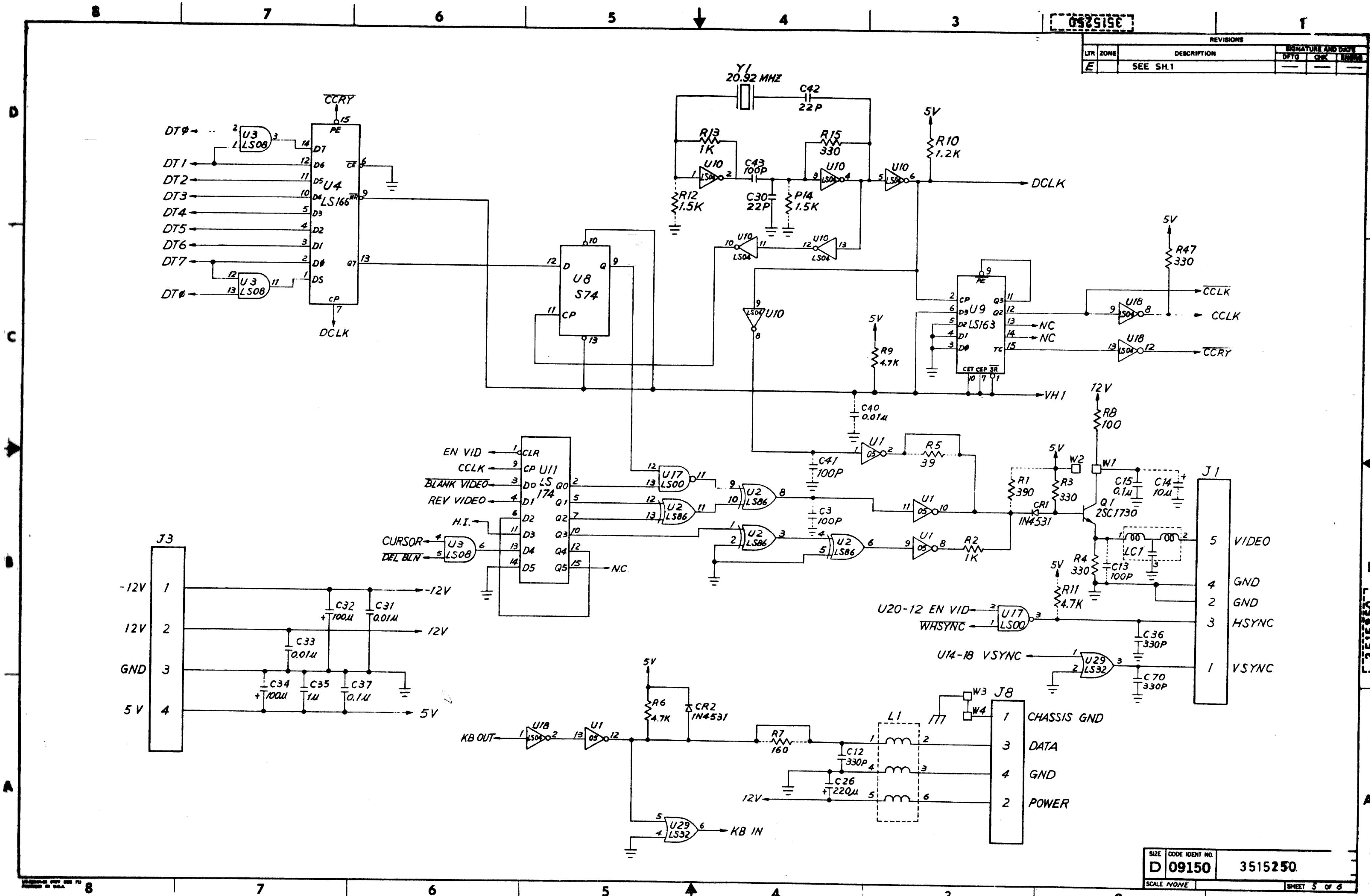
—	—	—	—
COMP. SIDE	SOLDER SIDE	COMP. SIDE	SOLDER SIDE
CUT TRCE		ADD JUMPER	

CUT TRACE AND JUMPER WIRE LIST (FOR -02 ONLY)

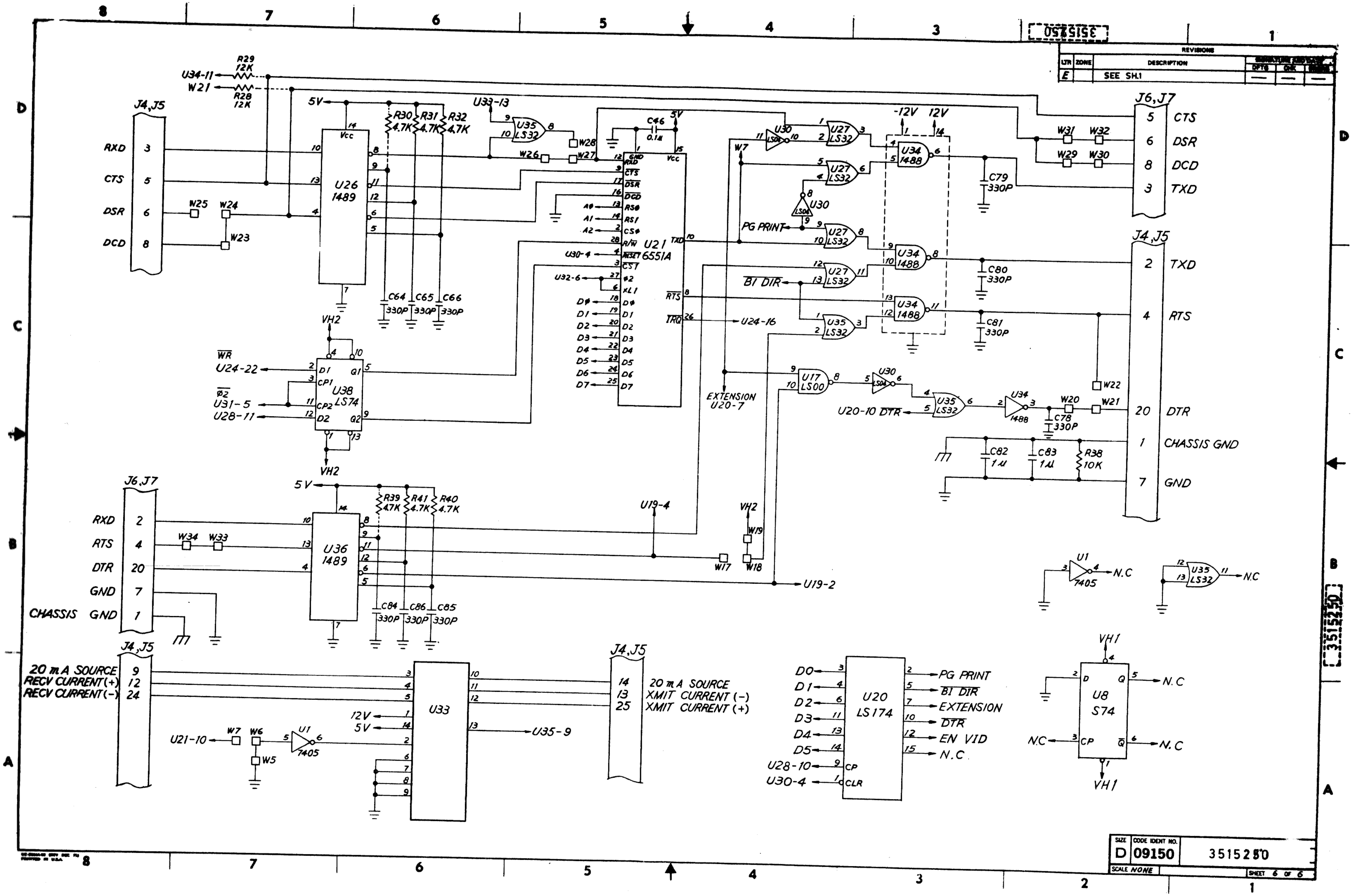
SIZE	CODE IDENT NO.	
D	09150	3515250
SCALE: NONE		SHEET 2 OF 6


3515250
REVISIONS
LTR | ZONE | DESCRIPTION | SIGNATURE AND DATE
E | SEE SH.1
D0~D7 DATA BUS
U24 Z80A
U23 2764
U22 2764
U25 TC5517 APL
U31 LS74
U28 LS139
U19 LS244
U37 NE555
Y2 3.6864MHZ
C75 22P
C74 .001μ
C49 1μ
C50 .022μ
C51 1μ
C54 2000P
C60 .01
C61 .01
C87 0.1μ
C88 0.1μ
C89 0.1μ
R33 820
R34 820
R35 330
R36 330
R37 4.7K
R19 4.7K
R46 4.7K
R45 2.2K
R44 1M
R43 100K
R42 100K
R16 33
R17 330
R18 1K
R21 1K
R22 2.2K
R23 180
R24 1K
R25 1.8K
R26 750
R27 1K
CR3 IN4531
CR4 IN4531
CR5 IN4531
CR6 IN4531
CR7 IN4531
CR8 IN4531
B1 3V
Q3 2N3644
Q4 2N3643
Q5 2N3643
REFERENCE DESIGNATION
COMPONENT | LAST USED | NOT USED
I. C. | U40 |
CAPACITOR | C89 | C20, C29
RESISTOR | R47 |
RESISTOR PACK | RP2 |
DIODE | CR8 |
TRANSISTOR | Q5 |
CRYSTAL | Y2 |
JUMPER HOLE | W34 |
INDUCTOR | L1 |
BATTERY | B1 |
JACK CONNECTOR | J8 | J2
FILTER | LC1 |
SIZE D | CODE IDENT NO. 09150 | 3515250
SCALE NONE | SHEET 5 OF 6


REVISIONS
LTR ZONE DESCRIPTION
E SEE SH.1
3515250
U14 2672
U15 2016
U13
U12 LS174
U7 LS174
U6 LS174
U5 2732 (2332)
U18
RP1
RP2
C25 0.1μ
C27 0.01μ
C9 0.1μ
C59 .01
R20 4.7K
5V
VH2
GND
Vcc
U24-17 NMI
U24-21 RD
U28-12 CE
U24-22 WR
A0
A1
A2
INTR
LPS
CCLK
WREN
DADD0
DADD1
DADD2
DADD3
DADD4/LA0
DADD5/LA1
DADD6/LA2
DADD7/LA3
DADD8
DADD9
DADD10/UL
DADD11
WDB
RDB
CURSOR
BLANK
VSYNC
HSYNC
VSYNC U29-1
TOSEL
UL
REV VIDEO
BLANK VIDEO
H.I.
WHSYNC
KB IN
KB OUT
DATA BUS D0~D7
DADD10/UL
DADD4/LA0
DADD5/LA1
DADD6/LA2
DADD7/LA3
U13-23 U.L
NC.
DEL BLN U3-5
DT 0
DT 1
DT 2
DT 3
DT 4
DT 5
DT 6
DT 7
SIZE D
CODE IDENT NO. 09150
3515250
SCALE NONE
SHEET 4 OF 6



REVISIONS
LTR | ZONE | DESCRIPTION | SIGNATURE AND DATE DFTG | CHK
E | | SEE SH.1 | — | —
3515250
Y1 20.92 MHZ
C42 22P
R13 1K
R15 330
R10 1.2K
5V
U10 LS04
C43 100P
C30 22P
P14 1.5K
R12 1.5K
DCLK
CCRY
U4 LS166
PE CE CP
D7 D6 D5 D4 D3 D2 D1 DØ DS Q7
DTØ DT1 DT2 DT3 DT4 DT5 DT6 DT7 DTØ
U3 LS08
U8 S74
D Q CP
U9 LS163
CP D3 D2 D1 DØ PE Q3 Q2 Q1 TC CET CEP SR
NC
NC
R47 330
U18 LS04
CCLK
CCLK
CCRY
R9 4.7K
C40 0.01µ
VH1
12V
R8 100
U1 05
R5 39
C41 100P
C3 100P
U11 LS 174
CLR CP D0 D1 D2 D3 D4 D5 Q0 Q1 Q2 Q3 Q4 Q5
EN VID
CCLK
BLANK VIDEO
REV VIDEO
H.I.
CURSOR
DEL BLN
N.C.
U17 LS00
U2 LS86
R2 1K
W2
W1
R1 390
R3 330
CR1 1N4531
Q1 2SC1730
C15 0.1µ
C14 10µ
LC1
R4 330
C13 100P
R11 4.7K
J1
5 VIDEO
4 GND
2 GND
3 HSYNC
1 VSYNC
U20-12 EN VID
WHSYNC
C36 330P
U14-18 VSYNC
U29 LS32
C70 330P
J3
-12V 1
12V 2
GND 3
5 V 4
C32 100µ
C31 0.01µ
C33 0.01µ
C34 100µ
C35 1µ
C37 0.1µ
-12V
12V
5V
R6 4.7K
CR2 1N4531
KB OUT
R7 160
L1
C12 330P
C26 220µ
W3
W4
J8
1 CHASSIS GND
3 DATA
4 GND
2 POWER
KB IN
SIZE D
CODE IDENT NO. 09150
3515250
SCALE NONE
SHEET 5 OF 6


REVISIONS
LTR ZONE DESCRIPTION
E SEE SH.1
3515250
J4,J5
RXD 3
CTS 5
DSR 6
DCD 8
U26 1489
U36 1489
U21 6551A
U38 LS74
U33
U20 LS174
U8 S74
J6,J7
CTS 5
DSR 6
DCD 8
TXD 3
J4,J5
TXD 2
RTS 4
DTR 20
CHASSIS GND 1
GND 7
J6,J7
RXD 2
RTS 4
DTR 20
GND 7
CHASSIS GND 1
20 mA SOURCE 9
RECV CURRENT(+) 12
RECV CURRENT(-) 24
20 mA SOURCE 14
XMIT CURRENT (-) 13
XMIT CURRENT (+) 25
PG PRINT
BI DIR
EXTENSION
DTR
EN VID
N.C
SIZE D
CODE IDENT NO. 09150
3515250
SCALE NONE
SHEET 6 OF 6

JET 80 T (AMPEX 210)

STATUS LINE:

1:
CHAR FDX A210 SWD KBON MONOFF AUXOFF NUMER PROTOFF GFXOFF DSRON 01-01

2:
STATOFF NORVID UDLFLH JUMP LNATB DUPE KBCLICK KBRPT LWCS

3:
TIMEAM08:00 SAVENB SCROLLON WRAPON BELLOFF CR=CR

4:
HOST9600 DTR AUX9600 BIDIROFF BIT8=0 STOP1 PAROFF NOPARCHK FREQ65

5:
HEOL=Ö_ HEOM=ÖM AEOM=ÖF HEREIS=

VID ÄNDRING AV DESSA FUKTIONER TRYCK PÅ " SHIFT SETUP "

STEGA MED HJÄLP AV PILARNA

ÄNDRA MED HJÄLP AV MELLANSLAGS TANGENTEN

SPARA MED HJÄLP AV " SHIFT S "