

Pin	Native		Expansion I/O side		MAX80	ABC1600	Expansion memory side	
	ABC80	ABC800	ABC80	ABC800			ABC80	ABC800
A1	-12 V							
A2	0 V							
A3	RESIN#		NC?		RESIN#	BPCLK#	NC?	
A4	GND		NC?		GND		XMEMFL#	
A5	XMEMWR#	INT#	*1	*2	XMEMW80#	INT#	XMEMWR#	INT#
A6	D7							
A7	D6							
A8	D5							
A9	D4							
A10	D3							
A11	D2							
A12	D1							
A13	D0							
A14	NC					CSB#	A15	
A15	RST#		= INP7# *4		= RESET#		A14	
A16	STATUS#		= INP1#				A13	
A17	INP#		= INP0#				A12	
A18	C4#		= OUT5#				A11	
A19	C3#		= OUT4#				A10	
A20	C2#		= OUT3#				A9	
A21	C1#		= OUT2#				A8	
A22	OUT#		= OUT0#				A7	
A23	CS#		= OUT1# *5		= ???		A6	
A24	GND	NMI#	NC?	NC?	NMI#	NMI# *3		A5
A25		INP2#		INP2#	NC	OPS# = INP2#		A4
A26		XINPSTB#		XINPSTB#		TREN#		A3
A27		XOUTPSTB#		XOUTPSTB#		TRRQ#		A2
A28		XM#		XM#		PRAC#		A1
A29		RFSH#		RFSH#	NC	PREN#		A0
A30	RDY (WAIT#)							
A31	+5 V							
A32	+12 V							

B1	-12 V							
B2	0 V							
B3	GND	XMEMWR#	NC	XMEMWR#	XMEMW800#	XMEMWR#		
B4	XMEMFL#					GND	NC	
B5	$\Phi = 3 \text{ MHz Z80 clock } *6$						$\Phi = 3 \text{ MHz Z80 clock } *6$	
B6	GND	NC?	NC	NC	NC	NC	NC	NC
B7								
B8								
B9								
B10								
B11								
B12	XINT5# *3							
B13	INT#	GND	*2	GND	INT#	XINT2# *3		
B14	A15					XCSB2# *3		
B15	A14					XCSB3# *3		
B16	A13					XCSB4# *3		
B17	A12					XCSB5# *3		
B18	A11					NC	NC	NC
B19	A10							
B20	A9					EXP# *3	NC	NC
B21	A8							
B22	A7					BUSEN# *3		
B23	A6					DSTB#		
B24	A5					GND		
B25	A4							
B26	A3							
B27	A2							XM#
B28	A1							RFSH#
B29	A0							NC
B30	NC	MEMRQ#	NC	MEMRQ#	NC	DIRW/R#	MEMRQ#	
B31	+5 V							
B32	+12 V							

Power
Not intended for power
CPU to bus
Bus to CPU
Bus to CPU open collector *7
Bidirectional
No connection

- \*1 INT#, XMEMWR# or NC depending on jumpers
- \*2 INT# or NC depending on jumpers
- \*3 BUS0X only, others NC
- \*4 Hard reset, INP 7 (ABC80/800), or RESET instruction (ABC1600)
- \*5 OUT 1 on ABC80/800, but not ABC1600
- \*6 2.9952 MHz on ABC80, 3.0000 MHz on ABC800
- \*7 ABC1600: Unsure about open collector, tristate or push-pull  
MAX80: OC signals have independent direction control