CMOS-KLOCKA /JW

MICROELECTRONIC – MARIN

E 050 - 16 1 BIT CLOCK TIMER

DESCRIPTION

This C-MOS circuit may be used as a real time clock or as an absolute time-counter with battery back up and an external 32 KHz quartz as time-refence. The information transfer takes place serially on a 1-bit bi-directional I/O data line in synchronism with an external clock. Data-exchange is controlled by the chip-select-signal. The internal time-counting circuit operates at a minimum voltage of 1.5 V. When a second supply of 5 V is connected to another input terminal, all outputs are then available. All of the outputs are capable of driving one T.T.L. unit load. The data I/O line is tri-state to enable it to work in microprocessor type environments.

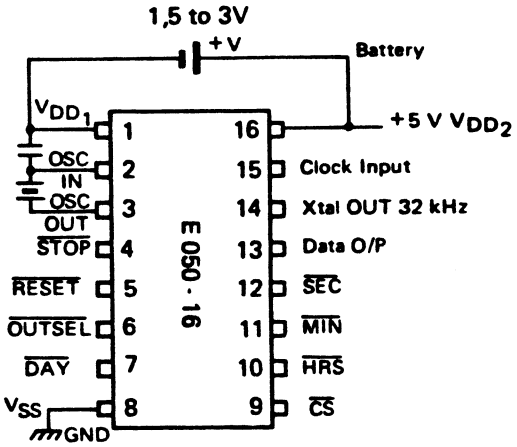
The data are in BCD format words.

FEATURES

- internal time-counter requires one external battery-cell only. Time is still running, even when supply-voltage is removed from circuit
- All of the outputs lines can drive one T.T.L. unit load with 5 V supply connected
- all input/time setting and output/time reading is performed through a single I/O-line for minimum wiring costs
- accepts low impedance 32 KHz-xtals as time reference
- choice of: a) read/write
  b) selected time information
  c) continuous reading of all time-data
- may be used in all µP-controlled or conventional electronic equipment, such as office calculators, electronic typewriters, industrial machine-control and TV-equipment or others
- counts seconds, minutes, hours, date of the month, day of the week, month and year
  every 4th year, February has 29 days
- available in a single 16 pin dual in-line package
- to write or read time-information, an external clock frequency of up to 150 KHz may be used.
- independent stop-input for external control of time-counting, for use as relative time-counter.
- may also be used as a preset time-counter, 24 hours by use of the time pulse outputs.
- easy connection to serial-in LCD-drivers to read out all time-data
- independent output-pins for second/minute/hour/day time-pulses
- Xtal frequency may be used to clock the data I/O and external circuits.

PACKAGE

16 Pin Dual in Line



Pin Connections and functions

1. V_{DD1} (Battery back up negative terminal)
2. OSC IN
3. OSC OUT
4. $\overline{STOP}$ (negative going I/P stop internal counting)
5. $\overline{RESET}$ (negative going I/P to reset)
6. $\overline{OUTSEL}$ (negative going I/P to read)
7. $\overline{DAY}$ (negative pulse every day)
8. VSS (GND)
9. $\overline{CHIP\ SELECT}$ (negative going I/P to start READ or WRITE FUNCTION)
10. $\overline{HRS}$ (negative pulse every hour)
11. $\overline{MIN}$ (negative pulse every minute)
12. $\overline{SEC}$ (negative pulse every second)
13. DATA IN/OUT
14. XTAL OUT 32 kHz
15. CLOCK (external frequency input)
16. VDD2 (positive supply + 5V)

OPERATION

BI-DIRECTIONAL DATA-TRANSFER (13)

Data-transfer to and from the chip is accomplished through a single I/O data-line (13), using external clock-pulses. (15) After the chip-select-input (9) has been activated (to a low level), a serial 3 bit address-word will first be accepted by the chip to select particular timing-information. A fourth bit selects read or write-mode, thus specifying whether the selected timing-information should be written into the circuit or read from it at pin 13 . Using the following clock-pulses, data-transfer with the chip at pin 13 may be accomplished.

When chip select is high the I/O line is high impedance, neither accepting nor giving out data.

Addressing the data

For serial data-transfer into or out of the chip, the address-data-line must first be activated by putting chip select to a low level.
When chip-select goes low the first 3 bits clocked into the chip by external clock-pulses will be interpreted as an address. This determines which time information is selected.

Adress-word	bit configuration MSB		LSB	selected time-information	counting capability
0	0	0	0	second	00...59
1	0	0	1	minute	00...59
2	0	1	0	hour	00...23
3	0	1	1	date	01...28/29.30/31
4	1	0	0	month	01...12
5	1	0	1	day of the week	01...07
6	1	1	0	year	00...99
7	1	1	1	continous data-transfer in the following sequence: hours, minutes, date, month, year, day of the week, seconds.	

Read/Write - select

The fourth bit clocked into the chip by external clock will decide whether the time information has to be read or written:

X X X 1 reads time information from the chip

X X X 0 writes time information into the chip to set the time.

Outsel (6)

If this input is set to logic "0" and if the "READ" mode is selected, the first bit of data will be sent onto the I/O PAD (13) at the negative edge of the 5 th clock pulse. When this input is left open or set to logic "1" the first bit of data is sent onto the I/O PAD (13) at the negative edge of the 4 th pulse.
(See timing diagrams)

Read-out mode

a) Selective data read-out (addresses 0...6)

If the I/P data at the positive edge of the 4th clock-pulses is "1" (for read), the selected time-data is sent from the internal time-counter into the output-shift-registers. The following 8 external negative edges will clock out 8 bit time data at pin 13 organized in two 4-bit BCD-format-words starting with the least-significant bit of the selected time-information. The time information is clocked out serially in synchronism with the negative edge of the external clock. All further clock-pulses are then ignored.

b) Continuous data read-out (address 7)

If the I/P data at the positive edge of the 4th clock-pulses is "1" (for read) and the address 7 was selected, all available time-information (from second to year) will be sent out with the following 56 external negative edges of the clock, i.e. in synchronism with the negative edge of the external clock. Data-transfer is then available in an 8 bit by 7 word serial format. The first bit of each time-data is again the least-significant bit.

If chip-select is kept at a low level (activated), the time data will be available every second, i.e. new timing-information is available once a second.
Interruption of dataflow is accomplished by returning chip-select to a high level state.

Write-in mode

a) Selective data write-in (addresses 0...6)

If the I/P data at the positive edge of the 4th clock-pulses is "0" (for write), time-information can be clocked into the chip via pin 13 by means of external clock-pulses at the clock I/P pin 15.

The following 8 external clock-pulses will clock the new timing information into the internal I/O shift register; all further clock-pulses are then ignored until chip-select goes high and then low again.
The first bit clocked into the chip, should be the most significant bit. The time-information is transfered from the internal I/O shift-register into the time-counting circuit with the rising edge of the chip-select signal; this defines the exact time at which the time information is updated.

b) Continuous data write-in (address 7)

This mode is similar to addresses 0...6, except that all 8 bit by 7 word time information is clocked into the chip in a predefined sequence; thus 60 clock-pulses are required for a complete cycle after chip-select goes low. Every 8 bit-word should be available in the format that the most significant bit is clocked in first. In this mode it is not necessary to return chip-select to a high level in order to write the information into the chip. This information is written into the chip only once for each low going chip-select-signal.

Chip-select (9).

Normally chip-select is high.

Chip-select going low enables the data I/O line, and allows all data to be clocked in synchronism with the external clock.

In the selective data write-in mode, the high going chip-select edge transfers the data from the internal I/O shift register into the time-counting network, thus specifying the exact time at which the time information is updated.

WHENEVER CHIP SELECT GOES HIGH THE I/O LINE (13) GOES INTO A HIGH IMPEDANCE STATE NEITHER ACCEPTING NOR GIVING OUT DATA.

Clock-In (15)

The positive going edge of the clock-signal controls address and data input. The negative going edge controls data output. The clock is internally gated by the chip-select-signal (9). Clock-pulses may be continuously connected to the chip-without shifting any data in or out- when chip-select is at a high level.

Address information will be clocked into the chip via pin 13 by the first 3 clock-pulses after chip-select goes low. At the fourth clock-pulses a decision is made whether the selected time-information should be read or written. The fifth and following clock-pulses will then clock-in or clock-out the time data. During selective read-write modes, the thirteenth and following clock-pulses are ignored until the next chip-select high-low excursion. During continuous read-write modes the 61st and following clock-pulses are also ignored until the next chip-select high-low excursion.

Power-on-reset

Upon connection of a battery between pins 1 and 16, an internal power-on-reset signal resets all counters to a specified condition. The O/P at the I/O pin (13) remains at a logic "1" until the chip-select pin (9) is taken low and then high again; after which the next chip-select can be used in the normal manner. This continuous logic "1" at the I/O pin indicates battery voltage has been removed at some time and that since this time the chip has never been accessed. This condition is a non-realistic time read out and can easily be detected by a μP as a power turn off signal.

Time counting commences as soon as the xtal starts oscillating.

Battery Operation (1,16)

A single cell battery must be connected between pins 1 and 16 of the package. This voltage keeps the internal time-counter running even when the 5 V supply is removed. The battery may be replaced by a chargeable cell and appropriate current limiting circuitry and charging of the battery can be accomplished by the 5 V supply.

$\overline{\text{Stop}}$ Input (4)

The circuit E 050/16 may also be used as a time-counter with start/stop operation.

When pin (4) is connected to logic "1" or left open circuit, the circuit will count time. When pin 4 is connected to logic "0" the circuit will stop counting time but will retain the most recent timing information.

$\overline{\text{Reset}}$-Input (5)

Reset of the internal time-counting is performed by a negative-going pulse at pin 5. When this pin is left open an internal pull-up resistor keeps the circuit in the counting mode. Reset to the individual registers is as shown:

00 second
00 minute
00 hour
01 date
01 month
01 day of the week
00 year

The WIDTH of the reset pulse should be not less than 14 uS. Time counting will remain static WHILST the reset input is low.

Time-Pulses Output (7, 10, 11, 12)

When $\overline{\text{Stop}}$-input (4) is left open or connected to a logic "1" continuous output timing-pulses are typically 32 μs wide and may be used to clock external circuitry every second, minute, hour or day, depending on the output-pin.

When address 7 is selected (continuous data), the pulse-length is automatically changed, it then becomes 56 clock-pulses long. The timepulse may then be used to gate or strobe the data from pin 13 into other external circuitry, i.e. display-drivers with serial data input. Timing-pulses will not be available, when $\overline{\text{stop}}$ (4) is at a low level. In order to return to 32 μs wide output pulses one of the selective data readouts must be performed.

32 KHz Output (14)

This output is connected via an internal driver directly from the xtal-oscillator.

This squareware may be used to clock external C.M.O.S. circuitry, i.e. serial-input display-drivers connected to the data-output pin. Pin 14 may be connected to clock-in (15) in order to clock the internal address and data I/O. Pin 14 may also be used to measure the xtal-frequency without loading the oscillator.

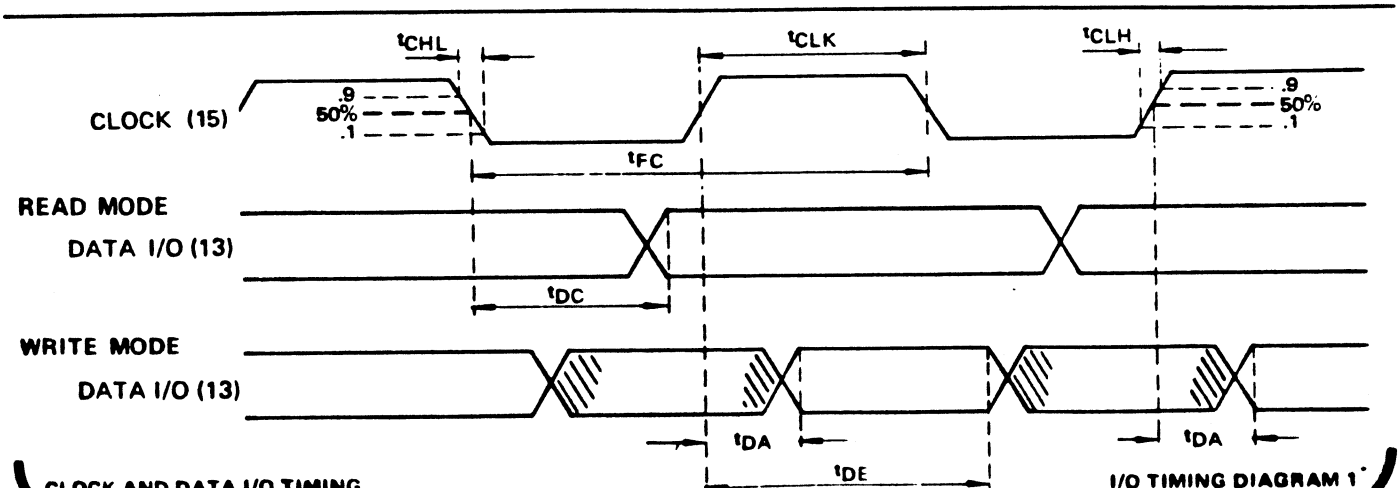
Supply-Voltage (16)

A supply-voltage of 5 V may be supplied at pin 16, in order to input or output time information. If this voltage is removed the internal time-counting still goes on when pin 16 has a battery-cell connected and when using the xtal time-base.

When this voltage is removed, all input- and output-levels (except the data I/O line) remain at the level of the +Ve line through internal pull-up resistors. Thus, no zero going time output-pulses are generated. The data I/O line is in a high impedance state without the 5 V supply connected.

Xtal (2+3) Quartz: f = 32 768 Hz
Rquartz = 40 kΩ typ, 60 kΩ max.
C_o = 1.5 pF
C_1 = 1.7 fF

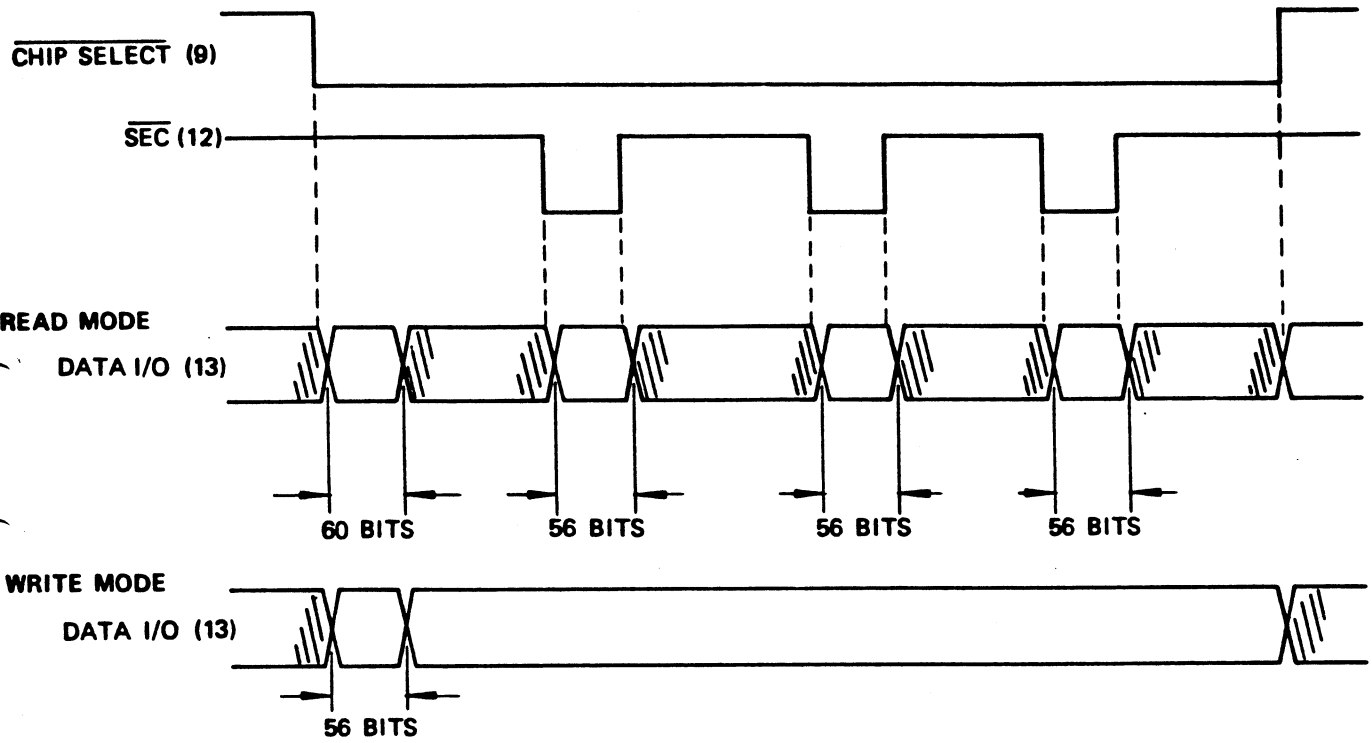
Frequency adjustment = ± 10 ppm Trimmer: C_T : 3 to 12 pF

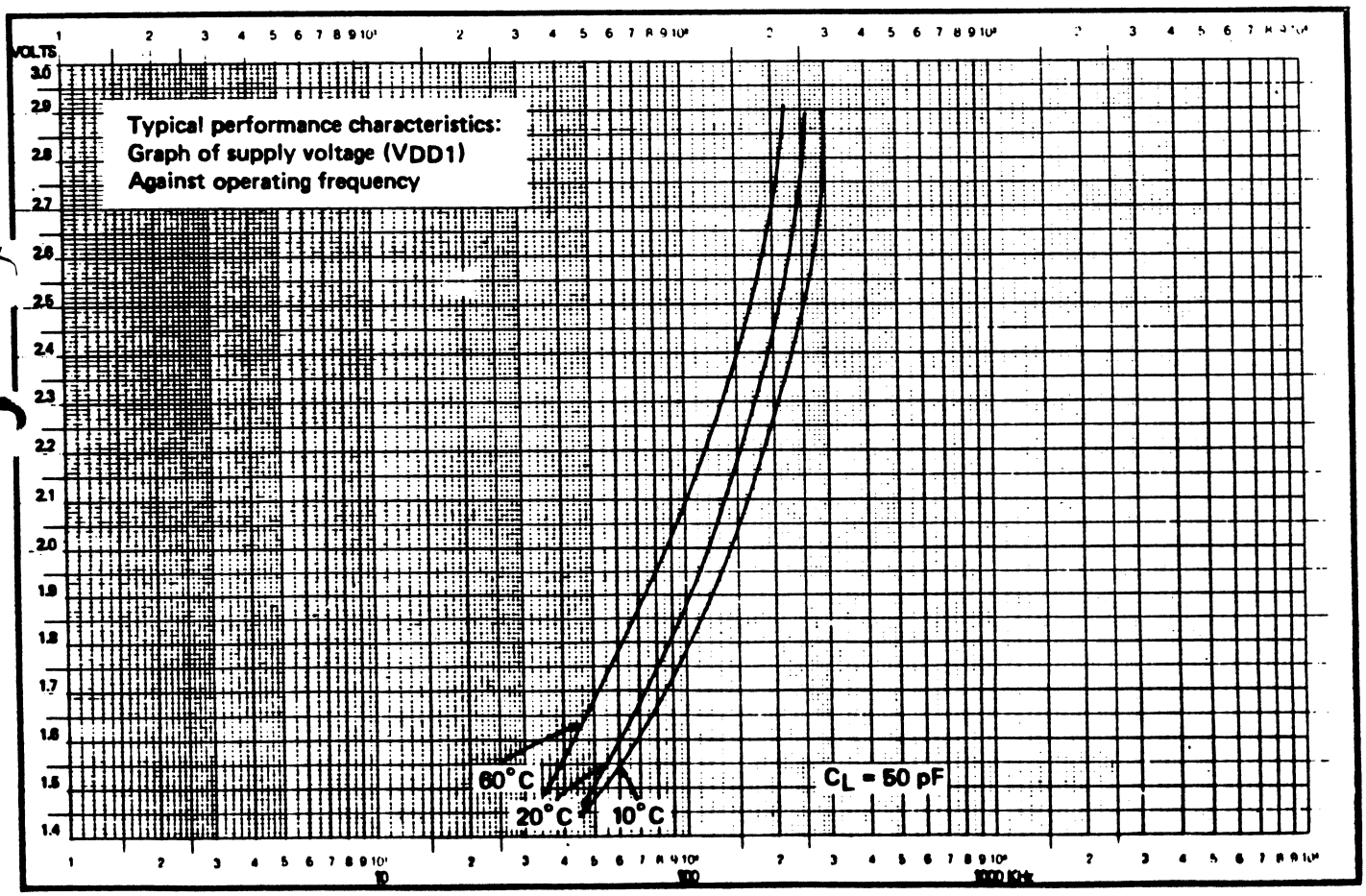


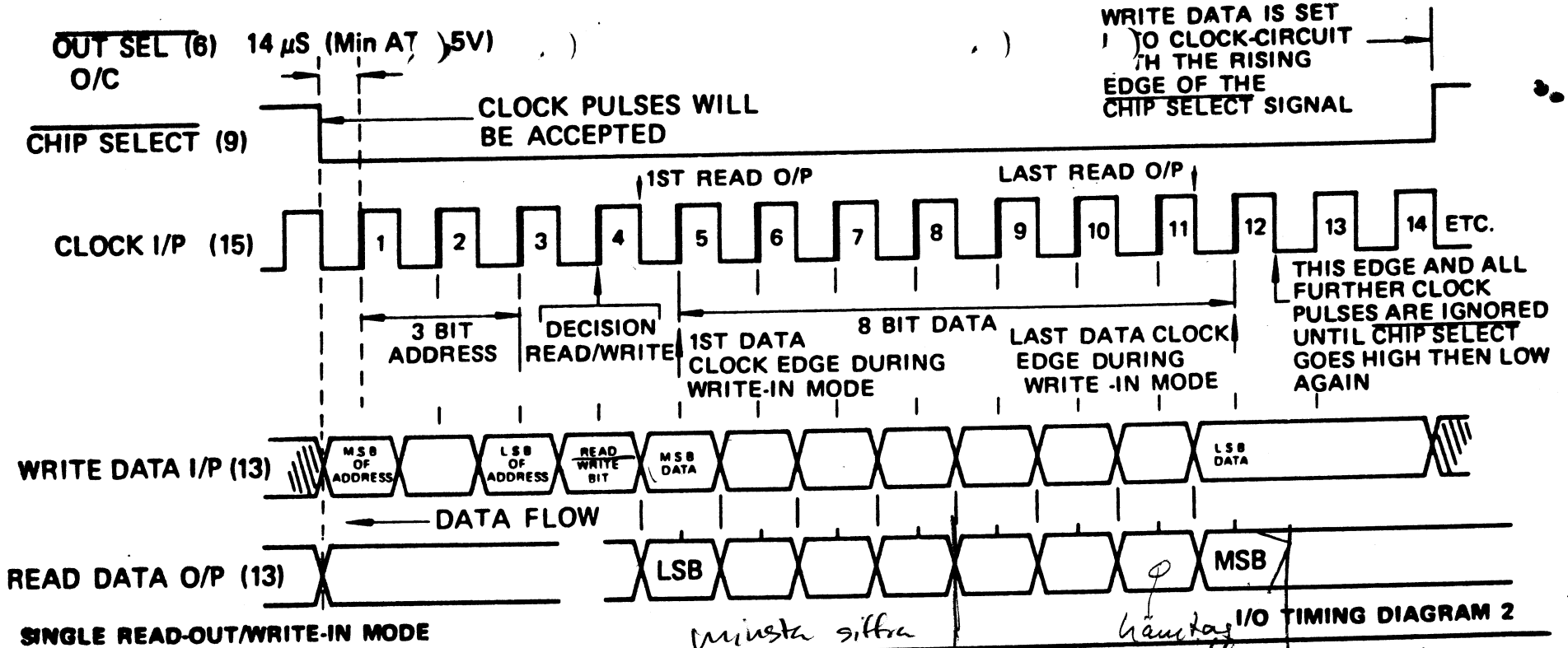
CLOCK AND DATA I/O TIMING

I/O TIMING DIAGRAM 1

CONTINUOUS READ-OUT/WRITE-IN MODE **I/O TIMING DIAGRAM 6**

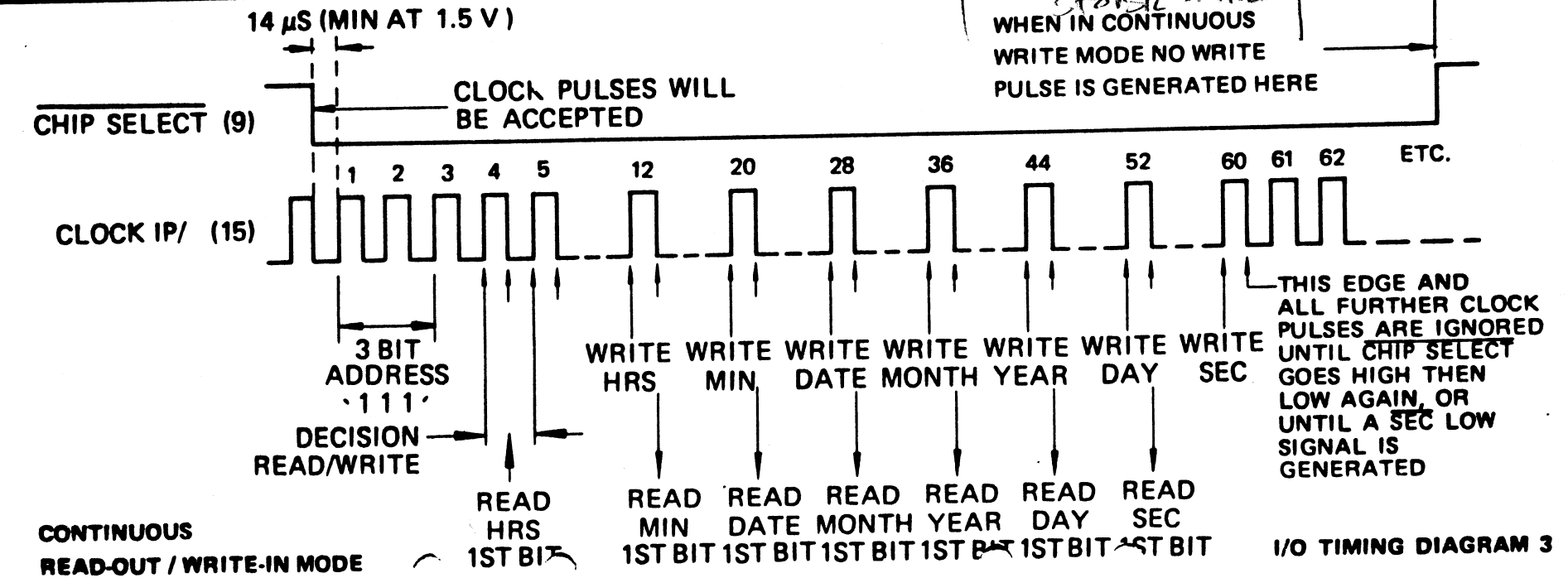






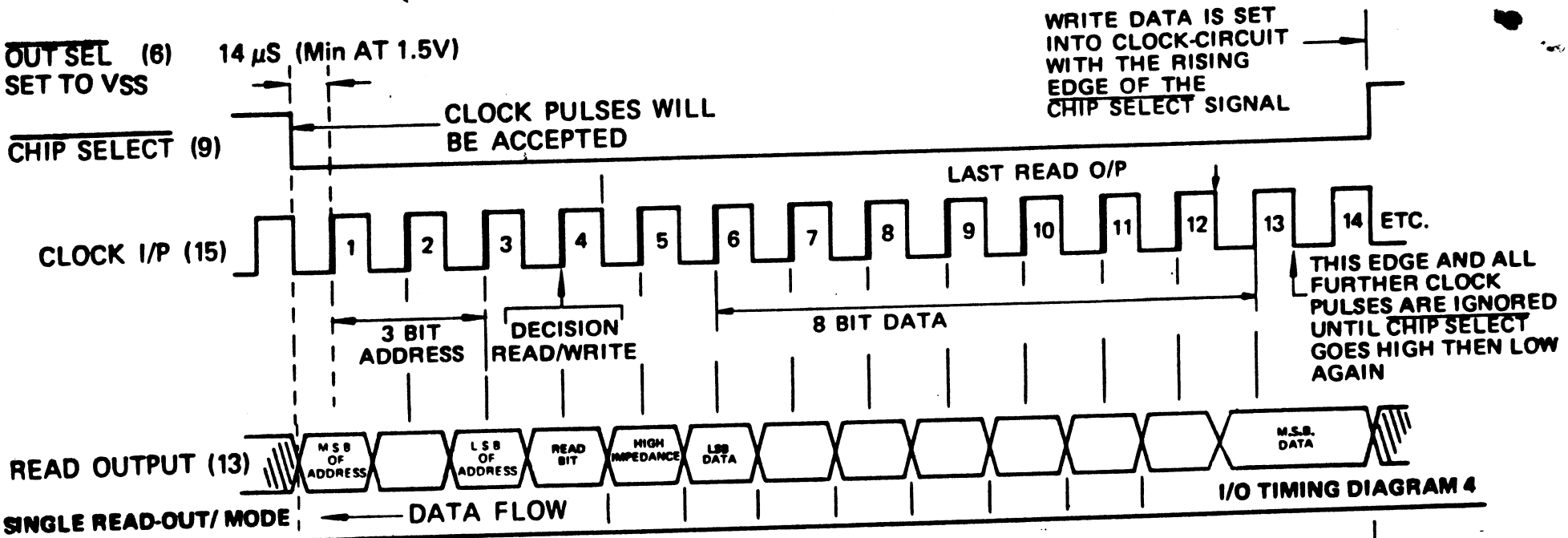
SINGLE READ-OUT/WRITE-IN MODE

I/O TIMING DIAGRAM 2

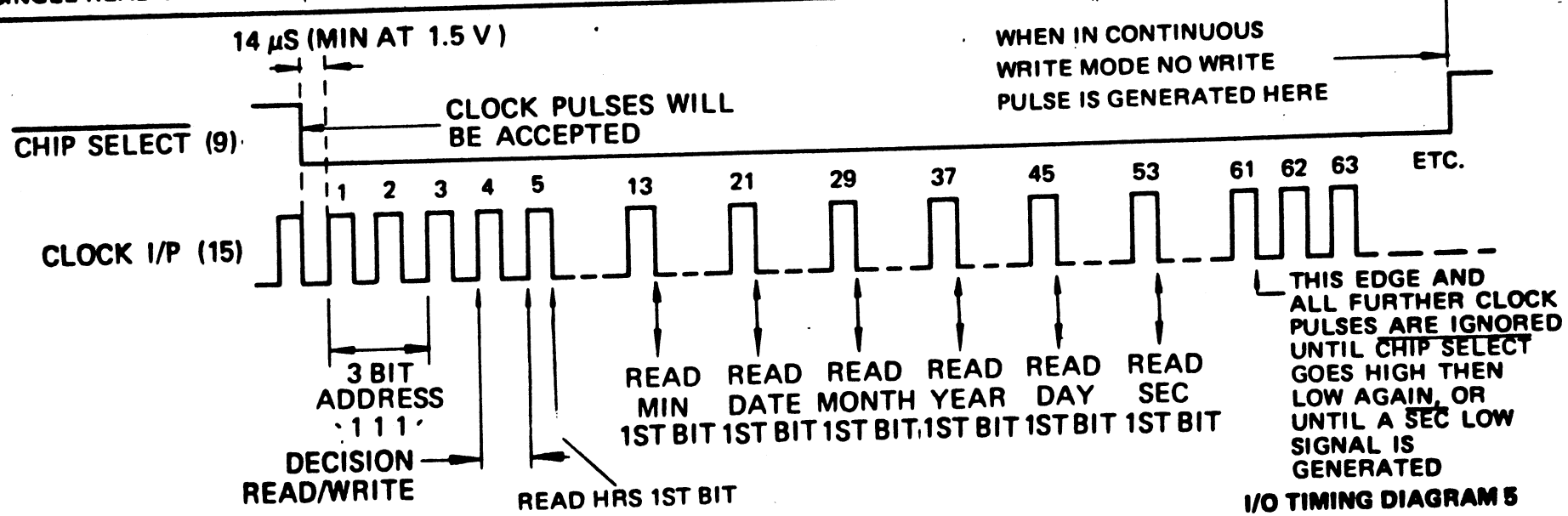


CONTINUOUS
READ-OUT / WRITE-IN MODE

I/O TIMING DIAGRAM 3



I/O TIMING DIAGRAM 4



I/O TIMING DIAGRAM 5