Signetics

SCN8031AH, SCN8051AH
Single-Chip 8-Bit Microcontroller

Product Specification

Microprocessor Products

DESCRIPTION

The Signetics SCN8031AH/8051AH is a high-performance microcontroller fabricated using Signetics' highly reliable +5V, depletion-load, N-channel, silicon-gate, N500 MOS process technology. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

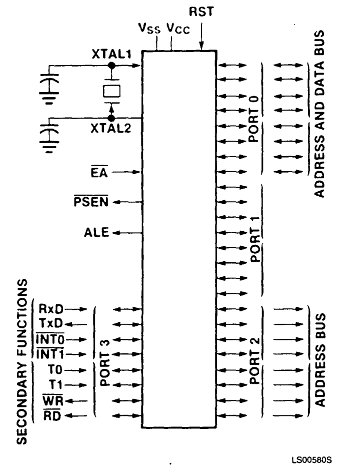
The SCN8051AH contains a 4K x 8 read-only program memory; a 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SCN8031AH is identical, except that it lacks the program memory. For systems that require extra capability, the SCN8051AH can be expanded using standard TTL compatible memories and byte oriented peripheral controllers.

The SCN8051AH microcontroller, like its SCN8048 predecessor, is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard SCN8048 instruction set are multiply, divide, subtract, and compare.

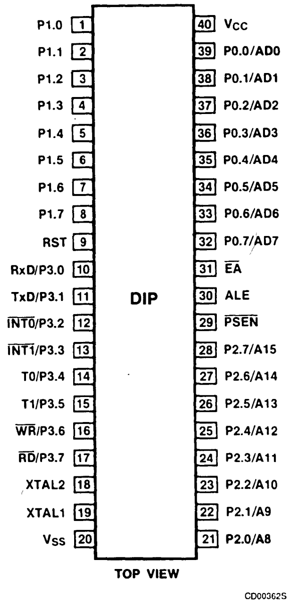
FEATURES

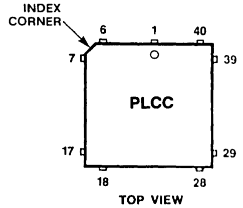
- **Reduced supply current**
- **4K x 8 ROM (SCN8051AH)**
- **128 x 8 RAM**
- **Four 8-bit ports, 32 I/O lines**
- **Two 16-bit timer/event counters**
- **High-performance full-duplex serial channel**
- **External memory expandable to 128K**
- **Boolean processor**
- **SCN80 series architecture enhanced with:**
  - **Non-paged jumps**
  - **Direct addressing**
  - **Four 8-register banks**
  - **Stack depth up to 128-bytes**
  - **Multiply, divide, subtract, compare**
- **Most instructions execute in 1μs**
- **4μs multiply and divide**

LOGIC SYMBOL



PIN CONFIGURATION





Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	A8/P2.0
3	P1.1	25	A9/P2.1
4	P1.2	26	A10/P2.2
5	P1.3	27	A11/P2.3
6	P1.4	28	A12/P2.4
7	P1.5	29	A13/P2.5
8	P1.6	30	A14/P2.6
9	P1.7	31	A15/P2.7
10	RST	32	$\overline{\text{PSEN}}$
11	RxD/P3.0	33	ALE
12	NC	34	NC
13	TxD/P3.1	35	$\overline{\text{EA}}$
14	$\overline{\text{INT0}}$/P3.2	36	AD7/P0.7
15	$\overline{\text{INT1}}$/P3.3	37	AD6/P0.6
16	T0/P3.4	38	AD5/P0.5
17	T1/P3.5	39	AD4/P0.4
18	$\overline{\text{WR}}$/P3.6	40	AD3/P0.3
19	$\overline{\text{RD}}$/P3.7	41	AD2/P0.2
20	XTAL2	42	AD1/P0.1
21	XTAL1	43	AD0/P0.0
22	V_{SS}	44	V_{CC}

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ORDERING CODE

SCN80□□ H □ □ □ 40 (CPxxxx)

ROM/RAM (bytes)
31 = EXT/128
51 = 4K/128

POWER CONSUMPTION
H = Reduced Power AH

OPERATING TEMPERATURE RANGE
A = −40°C to +85°C
C = 0°C to +70°C

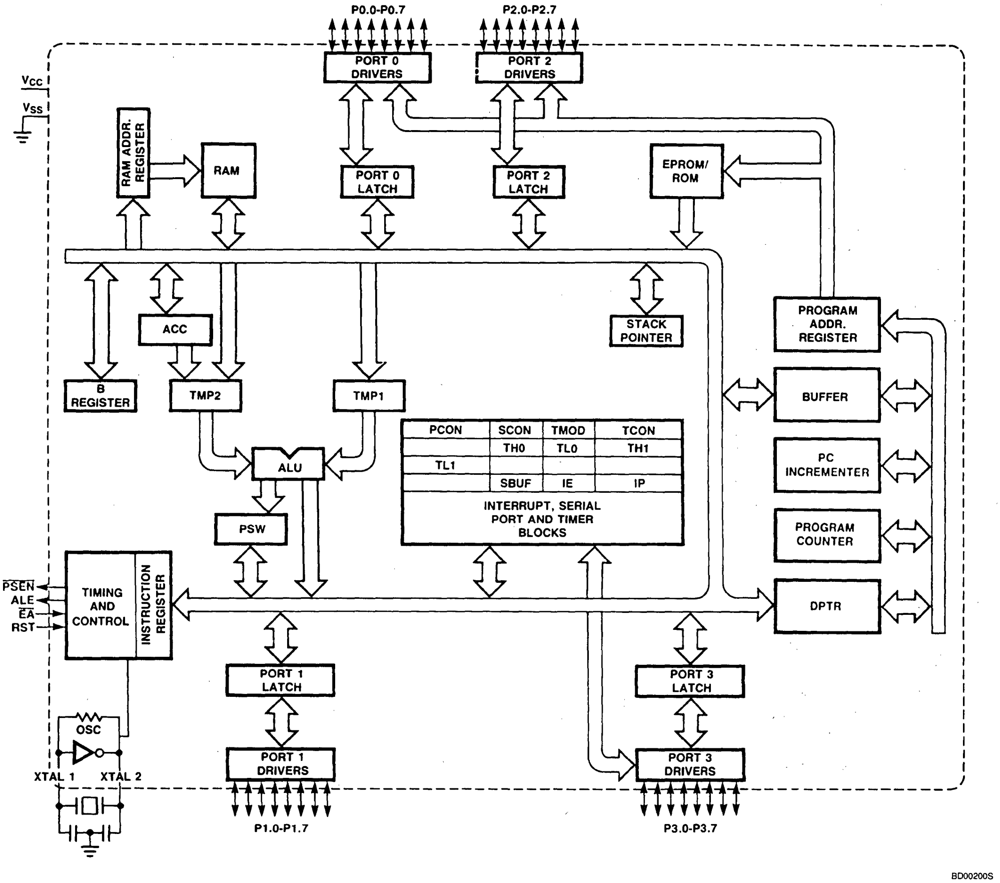
SPEED
C = 12MHz clock

CUSTOM ROM PATTERN NUMBER
Applies to masked ROM versions only. Number will be assigned by Signetics. Contact Signetics sales office for ROM pattern submission requirements.

40-PIN DIP
44-PIN PLCC

PACKAGE
N = Plastic DIP
I = Ceramic DIP
A = Plastic LCC

BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LCC		
V_{SS}	20	22	I	Circuit ground potential.
V_{CC}	40	44	I	Supply voltage during normal operation and program verification.
P0.0 - P0.7	39 - 32	43 - 36	I/O	**Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory. It also outputs instruction bytes during program verification. External pullups are required during program verification. Port 0 can sink (and in bus operation source) eight LS TTL inputs.
P1.0 - P1.7	1 - 8	2 - 9	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during program verification. Port 1 can sink/source three LS TTL inputs.
P2.0 - P2.7	21 - 28	24 - 31	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits and control signals during program verification. Port 2 can sink/source three LS TTL inputs.
P3.0 - P3.7	10 - 17	11, 13 - 19	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 can sink/source three LS TTL inputs. It also serves the functions of various special features as listed below. The output latch corresponding to a secondary function must be programmed to a logic 1 for that function to operate.
	10	11	I	RXD (P3.0): Serial input port
	11	13	O	TXD (P3.1): Serial output port
	12	14	I	$\overline{\text{INT0}}$ (P3.2): External interrupt 0
	13	15	I	$\overline{\text{INT1}}$ (P3.3): External interrupt 1
	14	16	I	T0 (P3.4): Timer 0 external input
	15	17	I	T1 (3.5): Timer 1 external input
	16	18	O	$\overline{\text{WR}}$ (P3.6): External data memory write strobe
	17	19	O	$\overline{\text{RD}}$ (P3.7): External data memory read strobe
RST	9	10	I	**Reset:** A high level on this pin for two machine cycles while the oscillator is running resets the device. An external pulldown resistor (≈8.2K) from reset to V_{SS} permits power-on reset using only a capacitor (≈10μF) connected from this pin to V_{CC}.
ALE	30	33	O	**Address Latch Enable:** Output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE pulse is skipped. ALE can sink/source eight LS TTL inputs.
$\overline{\text{PSEN}}$	29	32	O	**Program Store Enable:** Output is the read strobe to external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. (However, when executing out of external program memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external data memory.) $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. $\overline{\text{PSEN}}$ can sink/source eight LS TTL inputs.
$\overline{\text{EA}}$	31	35	I	**Instruction Execution Control:** When $\overline{\text{EA}}$ is held high, the CPU executes out of internal program memory (unless the program counter exceeds OFFFH). When $\overline{\text{EA}}$ is held low, the CPU executes only out of external program memory. $\overline{\text{EA}}$ must not be floated.
XTAL1	19	21	I	**Crystal 1:** Input to the inverting amplifier that forms the oscillator. This pin should be connected to V_{SS} when an external oscillator is used.
XTAL2	18	20	O	**Crystal 2:** Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. XTAL2 receives the oscillator signal when an external oscillator is used.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +7.0	V
Power dissipation	1.0	W

DC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC} = 4.5 to 5.5V, V_{SS} = 0V[4,5]

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
V_{IL} Input low voltage		-0.5	0.8	V
V_{IH} Input high voltage (except RST and XTAL2)		2.0	V_{CC} + 0.5	V
V_{IH1} Input high voltage to RST for reset, XTAL2	XTAL1 to V_{SS}	2.5	V_{CC} + 0.5	V
V_{OL} Output low voltage ports 1, 2, 3[6]	I_{OL} = 1.6mA		0.45	V
V_{OL1} Output low voltage port 0, ALE, $\overline{\text{PSEN}}$[6]	I_{OL} = 3.2mA		0.45	V
V_{OH} Output high voltage ports 1, 2, 3	I_{OH} = -80μA	2.4		V
V_{OH1} Output high voltage port 0, ALE $\overline{\text{PSEN}}$	I_{OH} = -400μA	2.4		V
I_{IL} Logical 0 input current ports 1, 2, 3	V_{IN} = 0.45V		-800	μA
I_{IH1} Input high current to RST for reset	$V_{IN} < V_{CC} - 1.5V$		500	μA
I_{LI} Input leakage current to port 0, $\overline{\text{EA}}$	$0.45 < V_{IN} < V_{CC}$		± 10	μA
I_{IL2} Logical 0 input current for XTAL2	XTAL1 = V_{SS}, V_{IN} = 0.45V		-2.5	mA
I_{CC} Power supply current	All outputs disconnected		125	mA
C_{IO} Capacitance of I/O buffer	f_C = 1MHz, T_A = 25°C		10	pF

T_A = -40°C to +85°C – Extended temperature range – SCN8051HAC only

V_{IH} Input high voltage (except RST and XTAL2)		2.2	V_{CC}+0.5	V
V_{IH1} Input high voltage to RST for reset, XTAL2	XTAL1 to V_{SS}	2.7		V
I_{CC} Power supply current	All outputs disconnected		175	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. For testing, all input signals swing between 0.45V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and at output voltages of 0.8V and 2.0V as appropriate.
6. V_{OL} is degraded when the SCN8031AH/SCN8051AH rapidly disch arges external capacitance. This AC noise is most pronounced during omission of address data. When using external memory, locate the latch or buffer as close to the SCN8031AH/SCN8051AH as possible.

Datum	Emitting Ports	Degraded I/O Lines	V_{OL}(Peak Max)
Address	P2, P0	P1, P3	0.8V
Write data	P0	P1, P3, ALE	0.8V

7. C_L = 100pF for port 0, ALE and PSEN outputs; C_L = 80pF for all other ports.

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V^{4,5,7}$

PARAMETER	12MHz CLOCK		VARIABLE CLOCK $1/t_{CLCL}$ = 3.5MHz to 12MHz		UNIT
	Min	Max	Min	Max	
Program memory char (fig. 1)					
t_{LHLL} ALE pulse width	127		$2t_{CLCL}$ −40		ns
t_{AVLL} Address set-up to ALE	43		t_{CLCL} −40		ns
t_{LLAX} Address hold after ALE	48		t_{CLCL} −35		ns
t_{LLIV} ALE to valid instr in		223		$4t_{CLCL}$ −100	ns
t_{LLPL} ALE to $\overline{PSEN}$	58		t_{CLCL} −25		ns
t_{PLPH} $\overline{PSEN}$ pulse width	215		$3t_{CLCL}$ −35		ns
t_{PLIV} $\overline{PSEN}$ to valid instr in		125		$3t_{CLCL}$ −125	ns
t_{PXIX} Input instr hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ} Input instr float after $\overline{PSEN}$		63		t_{CLCL} −20	ns
t_{PXAV} Address valid after $\overline{PSEN}$	75		t_{CLCL} −8		ns
t_{AVIV} Address to valid instr in		302		$5t_{CLCL}$ −115	ns
t_{PLAZ} $\overline{PSEN}$ to address float		25		25	ns
External data memory char (fig. 2 and 3)					
t_{RLRH} $\overline{RD}$ pulse width	400		$6t_{CLCL}$ −100		ns
t_{WLWH} $\overline{WR}$ pulse width	400		$6t_{CLCL}$ −100		ns
t_{LLAX} Address hold after ALE	48		t_{CLCL} −35		ns
t_{RLDV} $\overline{RD}$ to valid data in		250		$5t_{CLCL}$ −165	ns
t_{RHDX} Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ} Data float after $\overline{RD}$		97		$2t_{CLCL}$ −70	ns
t_{LLDV} ALE to valid data in		517		$8t_{CLCL}$ −150	ns
t_{AVDV} Address to valid data in		585		$9t_{CLCL}$ −165	ns
t_{LLWL} ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$ −50	$3t_{CLCL}$ +50	ns
t_{AVWL} Address to $\overline{WR}$ or $\overline{RD}$	203		$4t_{CLCL}$ −130		ns
t_{WHLH} $\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL} −40	t_{CLCL} +40	ns
t_{DVWX} Data valid to $\overline{WR}$ transition	23		t_{CLCL} −60		ns
t_{QVWH} Data set-up before $\overline{WR}$	433		$7t_{CLCL}$ −150		ns
t_{WHQX} Data hold after $\overline{WR}$	33		t_{CLCL} −50		ns
t_{RLAZ} Address float after $\overline{RD}$		25		25	ns
External clock (fig. 4)					
t_{CLCL} Oscillator period			83.3	286	ns
t_{CHCX} High time			20		ns
t_{CLCX} Low time			20		ns
t_{CLCH} Rise time				20	ns
t_{CHCL} Fall time				20	ns

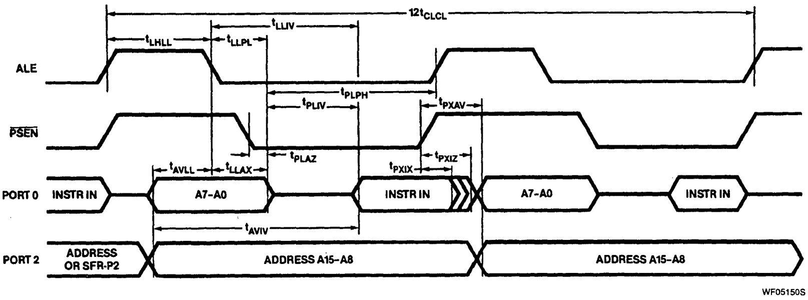

Figure 1. Program Memory Read Cycle

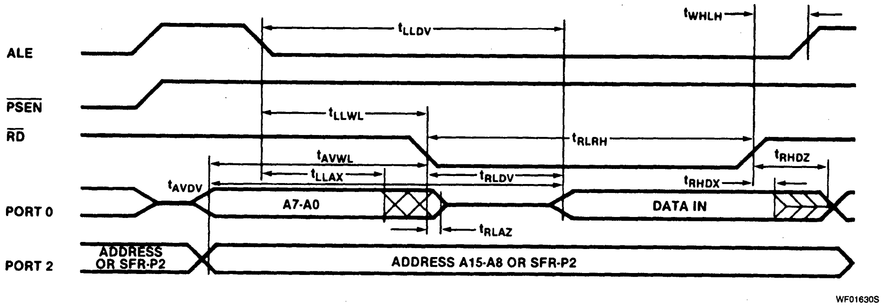

Figure 2. Data Memory Read Cycle

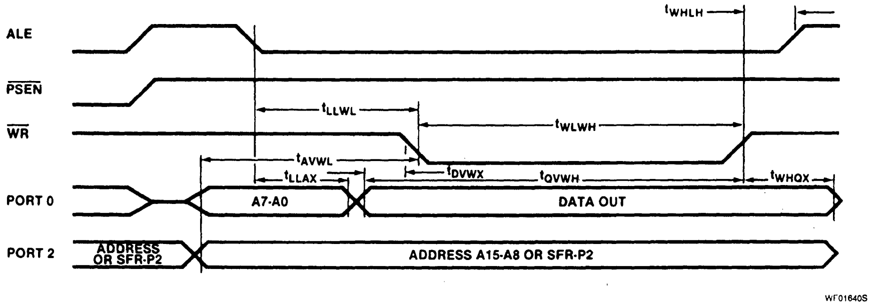

Figure 3. Data Memory Write Cycle

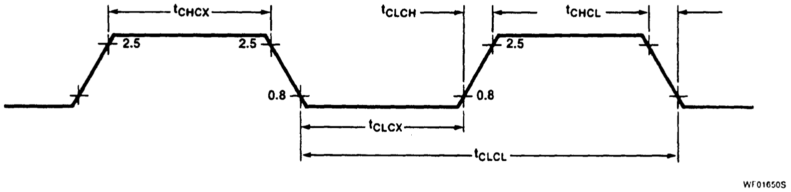

Figure 4. External Clock Drive XTAL2

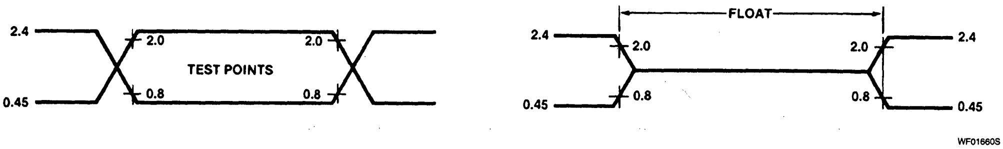

Figure 5. AC Testing Input/Output, Float Waveforms

NOTES:

1. AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
2. Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
3. For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400μA at the voltage test levels.

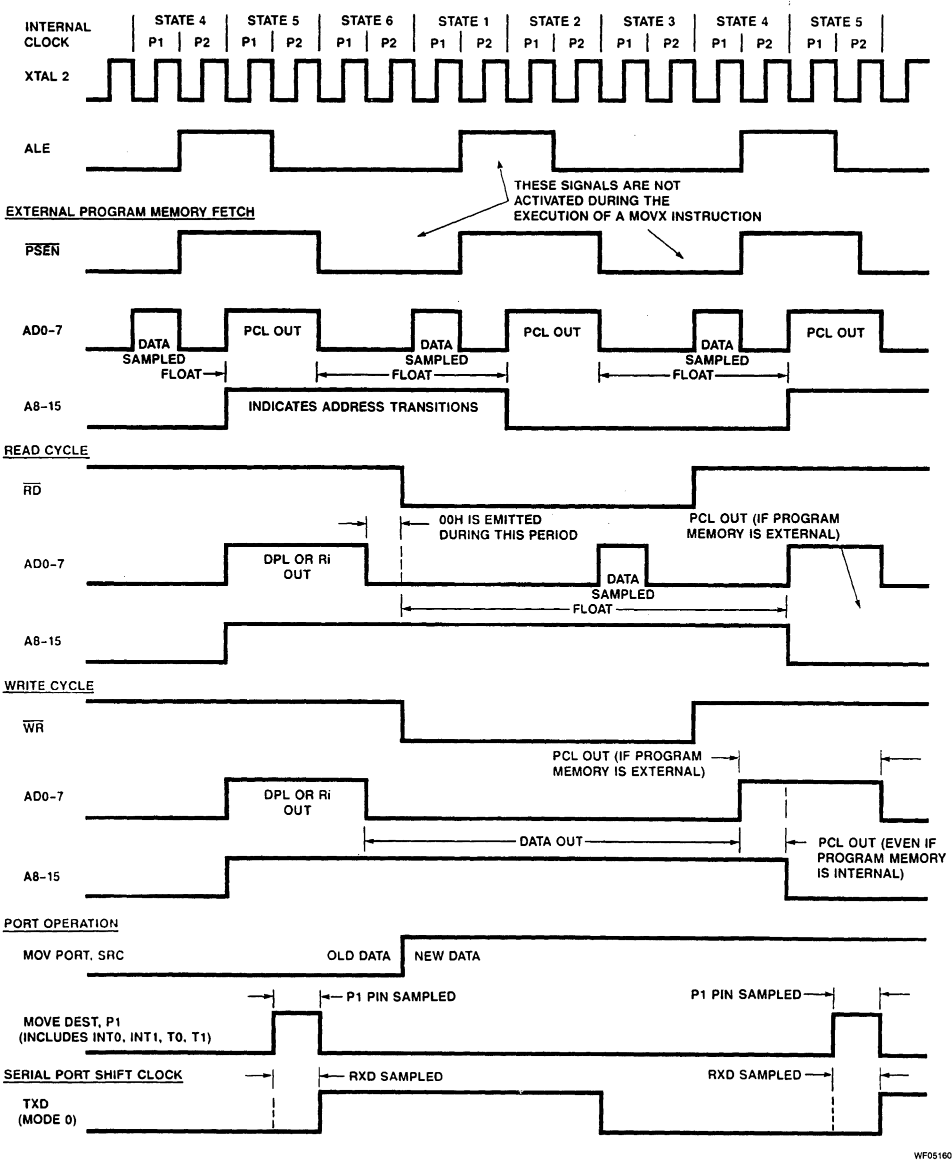

Figure 6. Timing Waveforms

NOTE:
All internal timing is referenced to the internal time states shown at the top of the page. This waveform represents the signal on the X2 input of the oscillator. This diagram represents when these signals are actually clocked within the chip. However, the time it takes a signal to propagate to the pins is in the range of 50-150ns. Propagation delays are dependent on many variables, such as temperature and pin loading. Even the different signals vary. Typically though, $\overline{RD}$ and $\overline{WR}$ have propagation delays of approximately 50ns and the other timing signals approximately 85ns. At room temperature, fully loaded, these differences in propagation delays between signals have been integrated into the timing specs.

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Table 1. INSTRUCTION SET

MNEMONIC		DESCRIPTION	BYTE	CYCLES
Arithmetic Operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,R#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/borrow	1	1
SUBB	A,#data	Subtract immed. data from A w/borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement Indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Mulitiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical Operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through the carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data Transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct, #data	Move immediate data to direct byte	3	2

Table 1. INSTRUCTION SET (Continued)

MNEMONIC		DESCRIPTION	BYTE	CYCLES
Data Transfer (Continued)				
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+ DPTR	Move code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM w/A	1	1
Boolean Variable Manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2
Program and Machine Control				
ACALL	addr11	Absolute subroutine call	2	2
LCALL	addr16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute jump	2	2
LJMP	addr16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if no carry flag	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set & clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & jump if not equal	3	2
CJNE	A,#data, rel	Comp. immed. to A & jump if not equal	3	2
CJNE	Rn,#data, rel	Comp. immed. to reg. & jump if not equal	3	2
CJNE	@Ri,#data, rel	Comp. immed. to ind. & jump if not equal	3	2
DJNZ	Rn,rel	Decrement register & jump if not zero	2	2
DJNZ	direct,rel	Decrement direct & jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn –Working register R0-R7
direct –128 internal RAM locations, any I/O port, control or status register
@Ri –Indirect Internal RAM location addressed by register R0 or R1
#data –8-bit constant included in instruction
#data16 –16-bit constant included as bytes 2 & 3 of instruction
bit –128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr16 –Destination address for LCALL & LJMP may be anywhere within the 64-kilobyte program memory address space.
addr11 –Destination address for ACALL & AJMP will be within the same 2-kilobyte page of program memory as the first byte of the following instruction.
rel –SJMP and all conditional jumps include an 8-bit offset byte. Range is +127–128 bytes relative to first byte of the following instruction.

Single-Chip 8-Bit Microcontroller SCN8031AH, SCN8051AH

Table 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr, code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr, code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	bit addr,code addr
31	2	ACALL	code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7

Table 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Continued)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr,A
43	3	ORL	data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr,A
53	3	ANL	data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	code addr
61	2	AJMP	code addr
62	2	XRL	data addr,A
63	3	XRL	data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data

Table 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Continued)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A + PC
84	1	DIV	AB
85	3	MOV	data addr,data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A + DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr

Table 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Continued)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A