		Pins				DIP												Programming address ranges
		18	19	20	21	1	2	3	4	5	6	7	8	9[x]	10	11	12	
256	Intel xx02	*Totally different pinout*				*Not supportable*												
512	Intel x704	$\overline{OE}$	+12V	$\overline{CE}$	-5V				■		■			X				7C00-7DFF
	Intel 33x4[orpd] Intel 36x4[opd]	CE4	CE3[‡]	$\overline{CE2}$	$\overline{CE1}$	■		■			■	■		X				7E00-7FFF
1K	Intel x608 Intel x708	$\overline{OE}$	+12V	$\overline{CE}$	-5V				■		■			X				7C00-7FFF
	Intel 2758	$\overline{CE}$	A_R[**]	$\overline{OE}$	V_{PP}[†]	[**]			■		■		†	X				
	Intel 36x8[o]	CE4	CE3[‡]	$\overline{CE2}$	$\overline{CE1}$	■		■			■	■		X				
	TMS2508	$\overline{CE}$	NC	$\overline{OE}$	V_{PP}[†]				■		■		†	X				
	TMS4700[r] Intel x308[r]	OE2[*]	+12V	$\overline{OE1}$	-5V			OE2	$\overline{OE2}$		■			X				
2K	Intel 2616 Intel 2716 TMS2516	$\overline{CE}$	A10	$\overline{OE}$	V_{PP}[†]				■		■		†	X		■		7800-7FFF
	TMS2716	$\overline{CE}$	+12V	A10	-5V				■						■			
	Intel 3636	CE3	CE2[‡]	$\overline{CE1}$	A10	■		■			■			X			■	7400-77FF 7C00-7FFF
	Intel x316[r]	*Totally different pinout*				*Not supportable*												
4K	2732[j]	$\overline{CE}$	A10	$\overline{OE}$	A11				■		■			X		■	■	7000-7FFF
	TMS2532	A11	A10	$\overline{CE}$	V_{PP}[†]		■				■		†	X		■		7000-73FF 7800-7BFF
	TMS4732[r]	A11	A10	CE1[*]	CE2[*]		■			CE1	$\overline{CE1}$	$\overline{CE2}$	CE2			■		7400-77FF 7C00-7FFF
8K	TMS4764[r]	A11	A10	$\overline{CE}$	A12		■				■			X		■	■	6000-67FF 7000-77FF 6800-6FFF 7800-7FFF
Programming		$\overline{CE}$	A10	$\overline{OE}$	A11				■					■		■	■	
						19	18	18	18	20	20	21	21	20	20	19	21	
						CE3	A12	CE1	$\overline{CE2}$	CE3	$\overline{CE4}$	$\overline{CE5}$	CE6	$\overline{OE}$	A10	A10	A11	

[p] Add pullup to pin 22 (A9) to support Intel 3304/3324/3604/3624

[d] Supporting Intel 3304/3324/3604 in the A-6 or AL version would require diode from pin 22 to Vcc

[‡] Add switches from pin 19 to handle CE (positive)

[**] A_R documented as “must be V_{IL} except on 2758 S1865 where is must be V_{IH}.” Extra OE?

[o] Part numbers x = 0 are open collector outputs; compatible if pulled up to Vcc. x = 2 is tristate

[r] Mask programmed ROM

[j] JEDEC standard, used by most vendors including Intel

[*] Programmable polarity – enable the correct switch for the part used

[†] V_{PP} can be used as extra positive OE for at least some vendors – see columns with †

[x] DIP 9 is don’t care if DIP 6 is closed